The 2011 International Conference on Integrated Circuits and Devices in Vietnam (ICDV 2011)

PROGRAM

Address: University of Engineering and Technology, Vietnam National University Hanoi
G3 building, 144 Xuan Thuy road, Cau Giay district, Hanoi, Vietnam

8-Aug-2011						
Session #1		**Location: 3-G3**		**Chairs: Masahiko YOSHIMOTO (Kobe University, Japan), Ngoc-Binh NGUYEN (UET, VNU, Vietnam)**		
START	**STOP**	**TIME**	**Type**	**Authors**	**Affiliation**	**Title**
9:00	**10:00**			**REGISTRATION**		
10:00	10:20	20	**Opening**	- Prof. Ngoc Binh NGUYEN* - Prof. Masahiko YOSHIMOTO** - Prof. Xuan-Tu TRAN*	*UET, VNU, Vietnam **Kobe University, Japan	- Opening speech 1 - Opening speech 2 - Introduction to ICDV 2011 program
10:20	11:20	60	**Keynote**	Kiyoo ITOH	Hitachi, Japan	Feasibility Study of 0.5-V High-Speed Memory-Rich Nanoscale CMOS LSIs
Cancel	Cancel	60	**Keynote**	Akira MATSUZAWA	Tokyo Institute of Technology, Japan	Ultra low-power analog/RF circuits and ADC design
11:20	12:00	40	***Special Talk - TJMW***	Kiyomichi ARAKI*, Yohei MORISHITA**	*Tokyo Institute of Technology, Japan, **Panasonic, Japan	A new type of receiver architecture suitable for SDR
12:00	**13:20**	**80**	**Lunch**			

Session #2		**Location: 3-G3**		**Chairs: Toshimasa MATSUOKA (Osaka University, Japan), Quang-Vinh TRAN (UET, VNU, Vietnam)**		
13:20	13:40	20	Oral	Trung-Kien NGUYEN*, Hoyong KANG*, In-Hwan LEE*, Cheol-Sig PYO*, and Chang-Wan KIM**	*Electronics and Telecommunications Research Institute, South Korea, **Dong-A University, Korea	RF CMOS Transceiver for 868/915 MHz Band IEEE802.15.4 Single-Chip
13:40	14:00	20	Oral	Trung-Sinh DANG, Anh-Dung TRAN, Min-Young CHO, Sang-Jin PARK, Sang-Woong YOON	Kyung Hee University, Korea	WLAN PA Efficiency Enhancement Using Buck Converter
14:00	14:20	20	Oral	Ikkyun JO*, Toshimasa MATSUOKA*, Takuji EBINUMA**	*Osaka University, Japan, **University of Tokyo, Japan	Design of Triple-band GPS CMOS Receiver
14:20	15:00	40	***Invited***	Shorin KYO, Shinichiro OKAZAKI	Renesas Electronics, Japan	Many-core Processors for Embedded Vision Applications
15:00	**15:20**	**20**	**Break**			
Session #3		**Location: 3-G3**		**Chairs: Fumio ARAKAWA (Renesas, Japan), Xuan-Tu TRAN (UET, VNU, Vietnam)**		
15:20	15:40	20	Oral	Duy-Hieu BUI, Xuan-Tu TRAN	University of Engineering and Technology, VNU, Vietnam	Multi-level Design Methodology using SystemC and VHDL for JPEG Encoder
15:40	16:00	20	Oral	Hanh Luyen DUC, Thien Le HA, Nhan Ngo THANH, Vinh Ngo QUANG	ICDREC, VNU-HCMC, Vietnam	MPEG-4 Decoder IP Verification Using Verification Methodology Manual
16:00	16:20	20	Oral	Thuan NGUYEN*, Thuan HUYNH*, Cong-Kha PHAM**	*Ho Chi Minh University of Science, Vietnam **University of Electro-Communications, Japan	An SoPC for Real-Time Motion Detection Using Spatial-Temporal Entropy
16:20	16:40	20	Oral	Quang Thieu HAN*, Chi Lan Phuong NGUYEN*, Nhat Van HUYNH**, Toyokazu HORI**	*Renesas Design Vietnam, Vietnam **Renesas Electronics, Japan	Effective and Easy Customization By RegBit Coverage In Video Input/Output IP
16:40	17:00	20	Oral	Van Tung LE*, Trong Tu BUI**	*University of Da Lat, Vietnam **University of Science, Vietnam	FPGA Implementation of An Audio Authentication Scheme
18:00	**20:30**	**150**	**Banquet**	**TRONG DONG restaurant (meeting point at E3 building)**		

9-Aug-2011						
Session #4		**Location: 3-G3**		**Chairs: Koichiro ISHIBASHI (University of Electro-Communications, Japan), Quang-Vinh TRAN (UET, VNU, Vietnam)**		
8:30	9:10	40	***Invited***	Francisco R. MADRIZ, Toshishige YAMADA, and Cary Y. YANG	Santa Clara University	High-frequency Characteristics of One-dimensional Nanostructures
9:10	9:30	20	Oral	Trung-Thanh LE	Hanoi University of Natural Resources and Environment, Vietnam	Arbitrary Power Splitting Couplers Based on Slot Nanophotonic Waveguides Using CMOS Technology
9:30	9:50	20	Oral	Pham Quoc TRIEU, Nguyen The NGHIA and Do Gia TUNG	Hanoi University of Science, VNU, Vietnam	Study on manufacture the device for detecting small magnetic field fluctuation
9:50	**10:10**	**20**	**Break**			
Session #5		**Location: 3-G3**		**Chairs: Akira TSUCHIYA (Kyoto University, Japan), Quang-Vinh TRAN (UET, VNU, Vietnam)**		
10:10	10:50	40	***Invited***	Nobuyasu KANEKAWA	Hitachi, Japan	Industrial Approach for Dependability in the Recent Decade
10:50	11:10	20	Oral	Tran Thuan HOANG, Dang Anh VIET, Tran Quang VINH	University of Engineering and Technology, VNU Hanoi, Vietnam	A 3D image capture system using a laser range finder for autonomous mobile robots
11:10	11:30	20	Oral	Phuc LE, Hoang Hau Nguyen THANH, Quoc Nguyen PHU	ICDREC, VNU-HCMC, Vietnam	Contact Smart Card Reader
11:30	11:50	20	Oral	Luu Manh HA, Tran Duc TAN, Chu Duc TRINH, Nguyen Thang LONG, Nguyen Dinh DUC	University of Technology and Engineering, VNU, Vietnam	INS/GPS Navigation for Land Applications via GSM/GPRS Network
11:50	**13:00**	**70**	**Lunch**			

Session #6		**Location: 3-G3**		**Chairs: Cong-Kha PHAM (University of Electro-Communications, Japan), Shorin KYO (Renesas Electronics, Japan)**		
13:00	14:00	60	***Keynote***	Thuong Cat PHAM	Institute of Information Technology, VAST, Vietnam	High Performance Parallel Computing using Cellular Neural Network on FPGA
14:00	14:20	20	Oral	Ngoc Hung NGUYEN, Xuan Thuan NGUYEN, Huu Thuan HUYNH, Trong Tu BUI	University of Science, VNU-HCMC, Vietnam	A Hardware Implementation of Pulse Coupled Neural Network for Image Feature Extraction
14:20	14:40	20	Oral	Manh Duong PHUNG, Thanh Van Thi NGUYEN, Quang Vinh TRAN	University of Engineering and Technology, VNU Hanoi, Vietnam	Control of an Internet-based Robot System Using Fuzzy Logic
14:40	15:00	20	Oral	Sergey CHURAYEV*, Timour PALTASHEV* and Victor STEMPITSKY**	*National Research University ITMO, Russia, **Belarusian State University of Informatics and Radioelectronics, Belarus	Effect of Lagging in Array of Ring Oscillators for On-Chip Digital Library Timing Verification
15h30	**18:30**	**120**	**Social Event**	**Visit Vietnam Museum of Ethnology**		

10-Aug-2011						
Session #7		**Location: 3-G3**		**Chairs: Dinh Viet NGUYEN (UET, VNU, Vietnam), Takeshi YAMAMURA (Fujitsu Lab., Japan)**		
8:30	9:30	60	***Keynote***	***Koichiro ISHIBASHI***	***University of Electro-Communications, Japan***	***Low Power Technologies and Their Impact on Societies***
9:30	10:10	40	***Invited***	Xuan-Tu TRAN	University of Engineering and Technology, VNU, Vietnam	Network-on-Chips: Design and Test Challenges in Nanoscale Era
10:10	10:30	20	Oral	Nam-Khanh DANG, Thanh-Vu LE-VAN, Xuan-Tu TRAN	University of Engineering and Technology, VNU, Vietnam	FPGA Implementation of a Low Latency and High Throughput Network-on-Chip Router Architecture
10:30	**10:50**	**20**	**Break**			
Session #8		**Location: 3-G3**		**Chairs: Dinh Viet NGUYEN (UET, VNU, Vietnam), Toshihiko HAMASAKI (Hiroshima Institute of Technology, Japan)**		
10:50	11:10	20	Oral	Vuong Dao VY, Do Van HUNG, Mai Truong GIANG, Hoa Quang DU, Nguyen Trong THE	University of Engineering and Technology, VNU, Hanoi, Vietnam	Designing and Manufacturing a Smart device
11:10	11:30	20	Oral	Chun Wei LIN, Sheng Feng LIN, Po Sheng LIN	National Yunlin University of Sci. and Tech., Taiwan	Design for Linear CMOS Temperature Sensor
11:30	11:50	20	Oral	Yong-Seo KOO*, Byung-Seok LEE*, Jin-Woo JUNG*, Dong-Su KIM*, Won-Suk PARK*, Yil-Suk Yang**	*University of Dankook, South Korea **Electronics and Telecommunications Research Institute, South Korea	Analysis of Dual-Directional SCR with low triggering voltage for I/O clamp
11:50	**13:00**	**70**	**Lunch**			

Session #9		**Location: 3-G3**		**Chairs: Ngoc-Binh NGUYEN (UET, VNU, Vietnam), Nobuyasu KANEKAWA (Hitachi, Japan)**		
13:00	14:00	60	***Keynote***	Masaharu IMAI, Takashi HAMABE, Yoshinori TAKEUCHI, and Keishi SAKANUSHI	Osaka University, Japan	Energy Reduction and Dependability Enhancement of Wireless Communication in Biomedical Information Sensing Systems
14:00	14:20	20	Oral	Son Hoang LE*, Phuong KIM*, Thi PHAM*, Thuyet That Vo NGUYEN*, Norio HAYASHI**	*Renesas Design Vietnam, Vietnam **Renesas Electronics, Japan	New RF front-end control interface from MIPI Alliance - Implementation for new MIPI RF front-end control interface
14:20	14:40	20	Oral	Quoc Tuan NGUYEN*, Duc Lap VU**	*University of Engineering and Technology, VNU, Vietnam **College of Poly-technique, Vietnam	Designed Synchronizations in Multi-Carrier Receivers on FPGA
14:40	15:00	20	Oral	Van-Phuc HOANG, Cong-Kha PHAM	University of Electro-Communications, Japan	Efficient LUT-based multiplier and squarer for DSP applications
15:00	**15:20**	**20**	**Break**			
Session #10		**Location: 3-G3**		**Chairs: Ngoc-Binh NGUYEN (UET, VNU, Vietnam), Pham Tuong HAI (Renesas Design Vietnam)**		
15:20	16:00	40	***Invited***	Fumio ARAKAWA	Renesas Electronics, Japan	Low Power Multicore for Embedded Systems
16:00	16:20	20	Oral	Van Huong PHAM, Ngoc Binh NGUYEN , Ngoc Hai BUI	University of Engineering and Technology, VNU, Vietnam	A Pareto Optimal Configuration at Design Phase for SoC Platform Based on the Genetic Algorithm
16:20	16:40	20	Oral	Duc-Hung LE*, Katsumi INOUE**, Masahiro SOWA*, Cong-Kha PHAM*	*University of Electro-Communications, Japan **Advanced Original Technologies, Japan	Implementation of Search-Less Information Detection based on Content Addressable Memory on FPGA
16:40	17:00	20	Oral	Tinh H. NGUYEN, Hoang M. TRAN, Minh D. NGUYEN	Hanoi University of Science and Technology, Vietnam	Verification Intellectual Property (VIP) for PCIe Compliance Verification
17:00	**17:20**	**20**	**Closing**	**Kunio UCHIYAMA* Ngoc-Binh NGUYEN****	***Hitachi, Japan ** UET, VNU, Vietnam**	