PROGRAM

The 6th International Conference on Integrated Circuits, Design, and Verification (ICDV 2015)

venue: Th	ne Universi	ty of Scienc	ce - vietnam	National University Ho Chi Minh city	r; 227 Nguyen Van Cu St., Ward 4, Distric	t 5, Ho Chi Minh City, Vietnam		
		Monday, August 10, 2015						
START 8:00	STOP 8:30	REGISTRAT	ION					
		REGISTRATION V Joint Plenary Session: Opening and Keynote Talks						
Room: Vung Tau (Conference Hall I)								
Co-chair: Xuan-Tu Tran, VNU University of Engineering and Technology, Vietnam								
Co-chair: Cong-Kha Pham, University of Electro-Communications, Japan								
START	STOP	Paper #	Туре	Author(s)	Affiliation(s)	Title		
8:30	8:35	-	-	Ngoc Binh Nguyen	Vietnam National University, Hanoi	Welcome Address by IEICE Vietnam Section		
8:35	8:40	-	-	Nguyen Van Hieu	HCM University of Science, Vietnam	Welcome Address by the hosting university		
8:40	8:45	-	-	Minoru Fujishima Kanji Itah	Hiroshima Univ., Japan	ICDV Opening Speech VJMW Opening Speeches		
8:45 8:50	8:50 9:00	- Photo Sess	-	Kenji Itoh	Kanazawa Inst. Tech., Japan	view Opening Speeches		
9:00	9:30	#47	Keynote	Huynh Cuong	HCM University of Technology, Vietnam	Design of A Short-Range X-Band FMCW Radar		
9.00	9.50		Reynote					
9:30	10:00	#26	Keynote	Kazuya Masu	Tokyo Institute of Technology, Japan	How to challenge in IoT-IoE era for LSI engineers		
10:00	10:20		Break & Post	ter Session & Booth				
MO2: ICD Room: Vu	V Session							
	-	Bui. Ho Ch	i Minh city l	Jniversity of Science, Vietnam				
			achi, Japan					
START	STOP	Paper #	Туре	Author(s)	Affiliation(s)	Title		
						Ultralow-Voltage Design and Technology of Silicon-on-Thin-		
10:20	10:50	#18	Invited	Shiro Kamohara	Renesas Electronics Corporation Japan	Buried-Oxide (SOTB) CMOS in IoT Era		
				Xuan-Thuan Nguyen, Hong-Thu	The University of Electro-Communications (UEC),			
10:50	11:10	#31	Oral	Nguyen, Trong-Thuc Hoang, Katsumi Inoue, Osamu Shimojo, Toshio	The University of Science (HCMUS),	DataBase Processor (DBP) - A New Search Engine for the Big		
10100			orui	Murayama, Kenji Tominaga, Cong-Kha	Advanced Original Technologies Co., Ltd (AOT),	Data Era		
				Pham	Nippon Computer Dynamics Co. Ltd (NCD)			
11:10	11:40	#24	Invited	Hitoshi Sugihara, Sao Noguchi, Kazunobu Morimoto, Pham Tuong Hai and Ichiro Naka	Renesas Electronics Corporation Japan, Renesas Design Vietnam	Renesas Design Vietnam – A Successful Model in Building-Up the Semiconductor Industry at Vietnam		
11:40	12:00	#40	Oral	Toan Nguyen Ngoc, Hung Cao Van, Quyet Hoang Van, My Nguyen Ngoc Phi, Tetsuya Shibayama, Seiji Mochizuki, Kenichi Iwata and Thang Minh Le	Renesas Design Vietnam & Renesas Electronics Corporation Japan	A 0.51ms Low-latency & Variant Bitrate H.264 Video Decoder for Surround View Monitoring and Car Infotainment		
12:00	13:30			1	LUNCH			
MO3: ICD	V Session	ll						
Room: Vu	ing Tau							
				f Engineering and Technology, Vietr	nam			
			University,					
START	STOP	Paper #	Туре	Author(s)	Affiliation(s)	Title		
13:30	14:00					Present Status of Characteristics Veriability in Advanced		
		#14	Invited	Toshiro Hiramoto	The University of Tokyo	Present Status of Characteristics Variability in Advanced MOSFETs		
14:00	14:30	#14 #23	Invited Invited	Toshiro Hiramoto Hanpei Koike, Masakazu Hioki, Yasuhiro Ogasahara, Hayato Ishigaki, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa	The University of Tokyo National Institute of AIST, Meiji University	· · ·		
14:00 14:30	14:30 15:00			Hanpei Koike, Masakazu Hioki, Yasuhiro Ogasahara, Hayato Ishigaki, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro		MOSFETs Flex Power FPGA and AlSTino A Design of Multi Channel Neural Recording Low-Noise Low-		
14:30	15:00	#23 #27	Invited Invited	Hanpei Koike, Masakazu Hioki, Yasuhiro Ogasahara, Hayato Ishigaki, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa	National Institute of AIST, Meiji University KEIO University	MOSFETs Flex Power FPGA and AlSTino		
14:30 15:00	15:00 15:30	#23 #27 #15	Invited Invited Invited	Hanpei Koike, Masakazu Hioki, Yasuhiro Ogasahara, Hayato Ishigaki, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa Nobuhiko Nakano Atsushi Muramatsu, Hong Gao, Hiroyuki Nakamoto	National Institute of AIST, Meiji University	MOSFETs Flex Power FPGA and AlSTino A Design of Multi Channel Neural Recording Low-Noise Low- Power Amplifier		
14:30 15:00 15:30	15:00	#23 #27 #15 Break & Pc	Invited Invited	Hanpei Koike, Masakazu Hioki, Yasuhiro Ogasahara, Hayato Ishigaki, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa Nobuhiko Nakano Atsushi Muramatsu, Hong Gao, Hiroyuki Nakamoto	National Institute of AIST, Meiji University KEIO University	MOSFETs Flex Power FPGA and AlSTino A Design of Multi Channel Neural Recording Low-Noise Low- Power Amplifier Thin and Flexible IoT-supporting Beacon Requiring No Battery		
14:30 15:00 15:30	15:00 15:30 15:50 V Session	#23 #27 #15 Break & Pc	Invited Invited Invited	Hanpei Koike, Masakazu Hioki, Yasuhiro Ogasahara, Hayato Ishigaki, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa Nobuhiko Nakano Atsushi Muramatsu, Hong Gao, Hiroyuki Nakamoto	National Institute of AIST, Meiji University KEIO University	MOSFETs Flex Power FPGA and AlSTino A Design of Multi Channel Neural Recording Low-Noise Low- Power Amplifier Thin and Flexible IoT-supporting Beacon Requiring No Battery		
14:30 15:00 15:30 MO4: ICD Room: Vu	15:00 15:30 15:50 V Session ing Tau	#23 #27 #15 Break & Pc	Invited Invited Invited oster Session	Hanpei Koike, Masakazu Hioki, Yasuhiro Ogasahara, Hayato Ishigaki, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa Nobuhiko Nakano Atsushi Muramatsu, Hong Gao, Hiroyuki Nakamoto	National Institute of AIST, Meiji University KEIO University	MOSFETs Flex Power FPGA and AlSTino A Design of Multi Channel Neural Recording Low-Noise Low- Power Amplifier Thin and Flexible IoT-supporting Beacon Requiring No Battery		
14:30 15:00 15:30 MO4: ICD Room: Vu Co-chair:	15:00 15:30 15:50 V Session Duc-Hung	#23 #27 #15 Break & Po	Invited Invited Invited Invited Ster Session	Hanpei Koike, Masakazu Hioki, Yasuhiro Ogasahara, Hayato Ishigaki, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa Nobuhiko Nakano Atsushi Muramatsu, Hong Gao, Hiroyuki Nakamoto & Booth	National Institute of AIST, Meiji University KEIO University	MOSFETs Flex Power FPGA and AlSTino A Design of Multi Channel Neural Recording Low-Noise Low- Power Amplifier Thin and Flexible IoT-supporting Beacon Requiring No Battery		
14:30 15:00 15:30 MO4: ICD Room: Vu Co-chair:	15:00 15:30 15:50 V Session Duc-Hung	#23 #27 #15 Break & Po	Invited Invited Invited Invited Ster Session	Hanpei Koike, Masakazu Hioki, Yasuhiro Ogasahara, Hayato Ishigaki, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa Nobuhiko Nakano Atsushi Muramatsu, Hong Gao, Hiroyuki Nakamoto & Booth Science, Vietnam	National Institute of AIST, Meiji University KEIO University	MOSFETs Flex Power FPGA and AlSTino A Design of Multi Channel Neural Recording Low-Noise Low- Power Amplifier Thin and Flexible IoT-supporting Beacon Requiring No Battery		
14:30 15:00 15:30 MO4: ICD Room: Vu Co-chair: Co-chair: START	15:00 15:30 15:50 V Session I Ing Tau Duc-Hung Hirofumi S	#23 #27 #15 Break & Pc	Invited Invited Invited University of Waseda Un	Hanpei Koike, Masakazu Hioki, Yasuhiro Ogasahara, Hayato Ishigaki, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa Nobuhiko Nakano Atsushi Muramatsu, Hong Gao, Hiroyuki Nakamoto & Booth Science, Vietnam iversity, Japan	National Institute of AIST, Meiji University KEIO University Fujitsu Laboratories Limited	MOSFETs Flex Power FPGA and AISTino A Design of Multi Channel Neural Recording Low-Noise Low- Power Amplifier Thin and Flexible IoT-supporting Beacon Requiring No Battery Replacements		
14:30 15:00 15:30 MO4: ICD Room: Vu Co-chair: Co-chair: START	15:00 15:30 15:50 V Session I Ing Tau Duc-Hung Hirofumi S STOP	#23 #27 #15 Break & Pc III Le, HCM L Shinohara, Paper #	Invited Invited Invited Invited Ster Session a University of Waseda Uni Type	Hanpei Koike, Masakazu Hioki, Yasuhiro Ogasahara, Hayato Ishigaki, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa Nobuhiko Nakano Atsushi Muramatsu, Hong Gao, Hiroyuki Nakamoto & Booth Cisence, Vietnam iversity, Japan Author(s) Yoshimasa Minami, Atsushi Watanabe,	National Institute of AIST, Meiji University KEIO University Fujitsu Laboratories Limited	MOSFETs Flex Power FPGA and AISTino A Design of Multi Channel Neural Recording Low-Noise Low- Power Amplifier Thin and Flexible IoT-supporting Beacon Requiring No Battery Replacements Title Bootstrap Charge Pump DC-DC Boost Converter using Multi		
14:30 15:00 15:30 MO4: ICD Room: Vu Co-chair: Co-chair: START 15:50	15:00 15:30 15:50 V Session Duc-Hung Hirofumi S STOP 16:10	#23 #27 #15 Break & Po III Le, HCM I hinohara, Paper # #3	Invited Invited Invited Invited Ster Session a University of Waseda Uni Type Oral	Hanpei Koike, Masakazu Hioki, Yasuhiro Ogasahara, Hayato Ishigaki, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa Nobuhiko Nakano Atsushi Muramatsu, Hong Gao, Hiroyuki Nakamoto & Booth Science, Vietnam iversity, Japan Author(s) Yoshimasa Minami, Atsushi Watanabe, Daichi Orihara and Nobuhiko Nakano Huong Nguyen, Giang Dang, Minh-Trien	National Institute of AIST, Meiji University KEIO University Fujitsu Laboratories Limited Affiliation(s) Keio University of Engineering and	MOSFETs Flex Power FPGA and AISTino A Design of Multi Channel Neural Recording Low-Noise Low- Power Amplifier Thin and Flexible IoT-supporting Beacon Requiring No Battery Replacements Title Bootstrap Charge Pump DC-DC Boost Converter using Multi Capacitors for Operating in Subthreshold Region Applying Improved Discrete PSO onto Mesh-based Network-on-		
14:30 15:00 15:30 MO4: ICD Room: Vu Co-chair: Co-chair: START 15:50 16:10	15:00 15:30 15:50 V Session Duc-Hung Hirofumi S STOP 16:10 16:30	#23 #27 #15 Break & Pc III Le, HCM L hinohara, Paper # #3 #45	Invited Invited Invited Invited Ster Session a University of Waseda Uni Type Oral Oral	Hanpei Koike, Masakazu Hioki, Yasuhiro Ogasahara, Hayato Ishigaki, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa Nobuhiko Nakano Atsushi Muramatsu, Hong Gao, Hiroyuki Nakamoto & Booth Science, Vietnam iversity, Japan Author(s) Yoshimasa Minami, Atsushi Watanabe, Daichi Orihara and Nobuhiko Nakano Huong Nguyen, Giang Dang, Minh-Trien Pham Yosuke Kuramoto, Jiro Ida Makoto Nagata, Kohki Taniguchi and	National Institute of AIST, Meiji University KEIO University Fujitsu Laboratories Limited Affiliation(s) Keio University VNU University of Engineering and Technology	MOSFETs Flex Power FPGA and AISTino A Design of Multi Channel Neural Recording Low-Noise Low- Power Amplifier Thin and Flexible IoT-supporting Beacon Requiring No Battery Replacements Title Bootstrap Charge Pump DC-DC Boost Converter using Multi Capacitors for Operating in Subthreshold Region Applying Improved Discrete PSO onto Mesh-based Network-on- Chip Application Mapping Evaluation of 0.2um SOI Based Super Steep Subthreshold Slope Device for Sensor and Ultra Low Power Applications Adaptive Suppression of Power Delivery Network Resonance		
14:30 15:00 15:30 MO4: ICD Room: Vu Co-chair: Co-chair: START 15:50 16:10 16:30	15:00 15:30 15:50 V Session I mg Tau Duc-Hung Hirofumi S STOP 16:10 16:30 16:50 17:20	#23 #27 #15 Break & Pc III Le, HCM U hinohara, Paper # #3 #45 #45 #7	Invited Invited Invited Invited Invited University of Waseda Uni Type Oral Oral Oral	Hanpei Koike, Masakazu Hioki, Yasuhiro Ogasahara, Hayato Ishigaki, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa Nobuhiko Nakano Atsushi Muramatsu, Hong Gao, Hiroyuki Nakamoto & Booth Science, Vietnam iversity, Japan Author(s) Yoshimasa Minami, Atsushi Watanabe, Daichi Orihara and Nobuhiko Nakano Huong Nguyen, Giang Dang, Minh-Trien Pham Yosuke Kuramoto, Jiro Ida Makoto Nagata, Kohki Taniguchi and Noriyuki Miura	National Institute of AIST, Meiji University KEIO University Fujitsu Laboratories Limited Affiliation(s) Keio University VNU University of Engineering and Technology Kanazawa Institute of Tehcnology Kobe University	MOSFETs Flex Power FPGA and AISTino A Design of Multi Channel Neural Recording Low-Noise Low- Power Amplifier Thin and Flexible IoT-supporting Beacon Requiring No Battery Replacements Title Bootstrap Charge Pump DC-DC Boost Converter using Multi Capacitors for Operating in Subthreshold Region Applying Improved Discrete PSO onto Mesh-based Network-on- Chip Application Mapping Evaluation of 0.2um SOI Based Super Steep Subthreshold Slope Device for Sensor and Ultra Low Power Applications Adaptive Suppression of Power Delivery Network Resonance with Chip-Package-Board Interaction		
14:30 15:00 15:30 MO4: ICD Room: Vu Co-chair: Co-chair: START 15:50 16:10 16:30 16:50	15:00 15:30 V Session I Ing Tau Duc-Hung Hirofumi S STOP 16:10 16:30	#23 #27 #15 Break & Pc III Le, HCM L hinohara, Paper # #3 #45 #7	Invited Invited Invited Invited Ster Session a Vaseda Uni Vaseda Uni Type Oral Oral Oral Oral	Hanpei Koike, Masakazu Hioki, Yasuhiro Ogasahara, Hayato Ishigaki, Toshiyuki Tsutsumi, Tadashi Nakagawa, Toshihiro Sekigawa Nobuhiko Nakano Atsushi Muramatsu, Hong Gao, Hiroyuki Nakamoto & Booth Science, Vietnam iversity, Japan Author(s) Yoshimasa Minami, Atsushi Watanabe, Daichi Orihara and Nobuhiko Nakano Huong Nguyen, Giang Dang, Minh-Trien Pham Yosuke Kuramoto, Jiro Ida Makoto Nagata, Kohki Taniguchi and	National Institute of AIST, Meiji University KEIO University Fujitsu Laboratories Limited Affiliation(s) Keio University VNU University of Engineering and Technology Kanazawa Institute of Tehcnology	MOSFETs Flex Power FPGA and AISTino A Design of Multi Channel Neural Recording Low-Noise Low- Power Amplifier Thin and Flexible IoT-supporting Beacon Requiring No Battery Replacements Title Bootstrap Charge Pump DC-DC Boost Converter using Multi Capacitors for Operating in Subthreshold Region Applying Improved Discrete PSO onto Mesh-based Network-on- Chip Application Mapping Evaluation of 0.2um SOI Based Super Steep Subthreshold Slope Device for Sensor and Ultra Low Power Applications Adaptive Suppression of Power Delivery Network Resonance		

Tuesday, 11 August 2015								
TU01: ICDV Session IV								
Room: Vung Tau								
Co-chair: Trong-Tu Bui, HCM University of Science, Vietnam								
Co-chair:	Akira Tsuc	hiya, Kyot	o University,	, Japan				
START	STOP	Paper #	Туре	Author(s)	Affiliation(s)	Title		
8:30	9:00	#28	Invited	Yuko Hara-Azumi, Tanvir Ahmed, Takuya Azumi, Nikil D. Dutt	Tokyo Institute of Technology	Instruction-Set Extension of Embedded Microprocessor for Timing Speculation		
9:00	9:20	#8	Oral	Yuuta Kunori, Jiro Ida	Kanazawa Institute of Tehcnology	Evaluation of Parasitic Capacitance in Gate Controlled Diode and Rectifier Circuit for High Efficiency RF Energy Harvesting		
9:20	9:40	#22	Oral	Tuan Anh Vu, Duong Bach Gia, Tor Sverre Lande	VNU University of Engineering and Technology	Non-Coherent IR-UWB Receiver Front-End for High-Precision Ranging and Localization		
9:40	10:00	#37	Oral	Phuoc Tran	VNU-HCM International University	A Compact Model for Linear, Nonlinear and Saturation Current in Graphene Field-Effect Transistors for RF Applications		
10:00	10:20		Break & Post	er Session & Booth	•			
TU02: ICD	V Session	v						
Room: Vu	ing Tau							
				f Engineering and Technology, Vietr	nam			
Co-chair:	Takeshi Sh	ima, Kana	gawa Unive	rsity, Japan				
START	STOP	Paper #	Туре	Author(s)	Affiliation(s)	Title		
10:20	10:50	#29	Invited	Ken Nakamura and Hiroe Iwasaki	NTT Media Intelligence Laboratories	Architecture of 8K Scalable HEVC encoder LSI		
10:50	11:10	#35	Oral	Tuan Nguyen-Viet, Duc-Hung Le	HCM University of Science	Selectable Register- and RAM-based TCAM Implementation using FPGAs		
11:10	11:40	#25	Invited	Hidetoshi Onodera	Kyoto University	Dependable VLSI Platform with Variability and Soft-Error Resilience		
11:40	12:00	#41	Oral	Tieu-Khanh Luong, Van-Phuc Hoang, Cong-Kha Pham	Le Quy Don Technical University, The University of Electro-Communications	An FPGA Implementation of OFDM System for IEEE 802.22 WRAN		
12:00	13:30				LUNCH			
TU03: ICD	V Session	VI						
Room: Vu	-							
				Engineering and Technology, Vietn	am			
Co-chair:	Jiro Ida, Ka I	anazawa U	niversity, Ja	pan I				
START	STOP	Paper #	Туре	Author(s)	Affiliation(s)	Title		
13:30	14:00	#19	Invited	Takeshi Shima, Nicodimus Retdian and Kento Takeuchi	Kanagawa University	New Design Methodologies for TDC and Programmable SC DC- DC Converter		
14:00	14:20	#46	Oral	Trung-Thanh Le	Vietnam National University, Hanoi	Fast and Slow Light Enhancement Based on Cascaded Microring Resonators Using the Sagnac Reflector on Silicon Waveguides		
14:20	14:50	#30	Invited	Kenshi Saho	Ritsumeikan University	Ultra Wideband Doppler Radar Signal/Image Processing for Human Motion Recognition		
14:50	15:10	#34	Oral	Toan Dao, Heisuke Sakai	Japan Advanced Institute of Science and Technology	Formation of Electrode Layer using Commercial Inkjet Printer for Bendable and Large-Area Electronics		
15:10	15:30				Break & Poster Session & Booth			
TU04: ICD	V Session	VII						
Room: Vu								
				Science, Vietnam				
Co-chair:	Cong-Kha	Pham, Uni	versity of El	ectro-Communications, Japan				
15:30	16:00	#43	Oral	Van-Khan Phan, Thanh-Huyen Do, Van- Phuc Hoang and Van-Lan Dao	Le Quy Don Technical University	An Energy-Efficient Wireless Sensor Network using ZigBee Standard		
16:00	16:20	#44	Oral	Ary Morales, William Polanco	FreeScale	Verification Bridge to Test High Speed Debug Interface for Automotive System in Package		
TU5: Closing								
Room: Vung Tau								
16:20	16:35		Closing	- Prof. Ngoc Binh Nguyen - Prof. Minoru Fujishima	IEICE Vietnam Section, VNU Hiroshima University	- Conference summary - Closing speech & Next Conference announcement		

POSTER PRESENTATIONS								
	10/08 10:00-10:20 10/08 15:30-15:50 - 11/08 10:00-10:20	#42	Poster	Toan Dao	Japan Advanced Institute of Science and Technology	Stretched-Exponential Distribution for Investigation of Stability of Tuned Threshold Voltage Organic CMOS		
		#10	Poster	Minh-Huan Vo, Ai-Quoc Dao	HCM University of Technical and Education	Dual Recycled Charge for Saving Leakage Power in Carry Look Ahead Adder for Low Power Applications		
		#33	Poster	Toan Dao	Japan Advanced Institute of Science and Technology	Controllable CMOS Circuits with Floating-Gate Like-based OTFT		
POSTER SESSIONS		#21	Poster	Thai Nguyen	ICDREC	The Implementation of Low Power, Cost Saving Decimation Filter in ICDREC Sigma-Delta 24-bit ADC		
		#32	Poster	Dinh-Tuan Pham, Dinh-Chinh Nguyen, Van-Vinh Pham, Ba-Cuong Doan, Duc- Tan Tran	VNU University of Engineering and Technology	Development of a Wireless Sensor Network for Indoor Air Quality Monitoring		
		#5	Poster	Thi Nguyen Duy Manh, Liem Giap Pham Hoang	HCM University of Science, Renesas Design Vietnam	Clock Tree Synthesis with Advanced Optimization Techniques		
		#39	Poster	Nhan Nguyen Huu	University of Information Technology	A Method For Vehicle License Plate Detection on FPGA Platform		