IEEE ICDV 2026 Program at a Glance

	Room A & Plenary Sessions	Room B
Time (Hanoi)	**Oct. 08**	
7:30-8:30	Registration	
8:30-8:50	Opening Session	
8:50-9:25	**Keynote 1: "Next-Generation IC Security: Resilient Hardware Design and AI-Enabled Forensic Verification"** *Prof. Bah-Hwee Gwee, Nanyang Technological University, Singapore*	
9:25-10:00	**Keynote 2: "Enforcing Security in the Supply Chain of Chiplets through Transparency"** *Dr. Sylvain Guilley, Cadence Design Systems and Telecom Paris, France*	
10:00-10:25	Coffee break & Expo	
10:25-11:55	**Session R1:** 5 papers/100 min Memory, digital systems and testing	**Session R2:** 5 papers/100 min AI, Quantum Tech. & Secure Autonomous UxV Systems
12:00-13:20	Lunch	
13:30-14:05	**Keynote 3: "Practical Non-Destructive Detection: Case Study of Durain, Mangosteen, and Granular Ingredients"** *Prof. Kosin Chamnongthai, King Mongkut's University of Technology Thonburi, Thailand*	
14:05-14:30	**Invited talk 1: Bridging the Gap Between Specification and Reality: Cellular Modem Development and Global Field Testing** *Prof. Chaehag Yi, Seoul National University, Korea*	
14:30-14:55	Coffee break & Expo	
14:55-16:15	**Session R3:** 4 papers/80 min FPGA and Embedded systems 1	**Session R4:** 4 papers/80 min Analog/mixed-signal circuits 1
16:55-18:15	**Session R5:** 4 papers/80 min Hardware security and cryptography 1	**Session R6:** 4 papers/80 min RF & microwave circuits
19:00-21:00	Gala Dinner	
	Oct. 09	
7:30-8:00	Registration	
8:00-8:35	**Keynote 4: "From Cloud Datacenters to Secure Edge: Review of Compute-in-Memory at EUV/FINFET Era"** *Prof. Koichiro Ishibashi, Universiti Teknologi Malaysia Kuala Lumpur (UTMKL), Malaysia*	
8:35-9:00	**Invited talk 2: "Open-Source EDA and PDKs in VLSI Design: The Era of Agentic AI, Maturing Ecosystems, and Democratized Silicon"** *Prof. Trong-Thuc Hoang, University of Electro-Communications, Japan & Prof. Van-Phuc Hoang, Le Quy Don Technical University, Vietnam*	
9:00-9:20	Coffee break & Expo	
9:20-9:50	**Invited talk 3: A Methodology to Derive Security Specifications for Complex Electronic Systems** *Sylvain Guilley (Telecom Paris & Cadence Design Systems, France), Ritu-Ranjan Shrivastwa and Ville Yli-Mayry (Cadence Design Systems, France)*	
9:50-11:50	**Session R7:** 6 papers/120 min AI, IoT & communications 1	**Session R8:** 6 papers/120 min FPGA and Embedded systems 2
11:50-13:10	Lunch	
13:15-13:50	**Keynote 5: "Hardware Accelerator Design and Optimization for Functional Encryption"** *Prof. Makoto IKEDA, Systems Design Lab (D.lab), Engineering School, The University of Tokyo, Japan*	
13:50-15:10	**Session R9:** 5 papers/100 min AI, IoT & communications 2	**Session R10:** 5 papers/100 min Analog/mixed-signal circuits 2

15:10-15:30	Coffee break & Expo	
15:30-17:10	**Session R11:** 5 papers/100 min Semiconductor Technology	**Session R12:** 5 papers/100 min Hardware security and cryptography 2
17:15-17:25	Closing	
	Oct. 10	
9:30-11:00	Committee Meeting	
12:00-18:00	Field trip	

Conference venue: 5F, S1 building, Le Quy Don Technical University, 236 Hoang Quoc Viet str., Nghia Do ward, Hanoi, Vietnam

Total talks: 65 (05 keynotes + 03 invited papers + 57 regular papers)