The 10th International Conference on Integrated Circuits, Design, and Verification (ICDV 2025)

The University of Science - Vietnam National University Ho Chi Minh City, 16-17 June, 2025

FINAL TECHNICAL PROGRAM

Day 1: 16 June 2025

Time	Title		Venue
8:30-9:00	Registration		Main hall, I building
9:00-9:10	Welcome speech (Prof. Tran Minh Triet, Vice President of HCMUS)		
9:10-9:20	Opening speech (Prof. Tran Xuan Tu - Director VNU-ITI)		
Keynote Speech (Chair: Prof. Tran Xuan Tu (Information Technoloy Insitute - VNU Hanoi), Assoc. Prof. Le Duc Hung(The University of Science - VNUHCM))			
9:20 - 10:05	Keynote #1: Advanced Biomedical Imaging Technologies: Circuit Design and Techniques	Prof. Yongfu Li (Shanghai Jiaotong University, China)	Main hall, I building
10:05 - 10:35	**Coffee break and networking**		
10:35 - 11:20	Keynote #2: Multi-core Multi-thread RISC-V-based System-on-Chip	Prof. Cong-Kha Pham (The University of Electro-Communications, Japan)	
11:30 - 13:30	**Lunch**		
13:30 - 14:45	**Technical session: Hardware Accelerator for AI (Chair: Dr. Bui Duy Hieu - Information Technoloy Insitute - VNU Hanoi)**		
13:30 - 13:45	An Optimized Obstructive Sleep Apnea Detection Model Using Particle Swarm Optimization and Machine Learning	Saroj Biswas; Atiya Khan; Chukhu Chunka (National Institute of Technology Silchar, India)	Room I23
13:45 - 14:00	An Optimized Hybrid Quantum-Classical Neural Network Model for Handwritten Digit Classification	Quoc Minh V. Nguyen; Trung-Khanh Le; Trong-Tu Bui; Duc-Hung Le (University of Science, VNU-HCM, Vietnam)	
14:00 - 14: 15	Harnessing TinyML for Accurate ECG Beat Detection	An Dong Bui (University of Science, VNU-HCM, Vietnam); Hoang Anh Vy Ngo (ITRVN, Vietnam); Dat Hoang Tran (ITRVN, Vietnam)	
14:15 - 14:30	FPGA-based Design and Implementation of Processing Element Array for Convolutional Neural Networks	Chi Phuong Hoang; Nguyen D. Minh; Linh Nguyen-Thi-Thuy; Luu Nguyen-Van (Hanoi University of Science and Technology, Vietnam)	
14:30 - 14:45	Efficient AI Model and Hardware Architecture Based on CNN for Arrhythmia Prediction	Huy Duc Pham (University of Science, VNU-HCM, Vietnam); Thi-Minh-Tuyen Huynh (University of Science, VNU-HCM, Vietnam); Tuan-Kiet Tran (University of Science, VNU-HCM, Vietnam); Thanh-Dat Bui (University of Science, VNU-HCM, Vietnam); Cong-Kha Pham (University of Electro-Communications, Japan); Huu-Thuan Huynh (University of Science, VNU-HCM, Vietnam)	
14:45 - 15:15	**Coffee break**		
15:15 - 16:30	**Technical session: Analog and Mixed-Signal Integrated Circuits (Chair: Dr. Bui Trong Tu - The University of Science - VNUHCM)**		
15:30 - 15:45	High-PSR Capacitor-Less LDO with Enhanced Bandgap Reference in 65nm CMOS Technology	Viet N. D Ngo; Cuong Huynh (Ho Chi Minh University of Technology, VNUHCM)	Room I23
15:45 - 16:00	Inductorless 5.405 GHz Fractional-N PLL for RF Synthesis with 5.6 mW Power Consumption	Ha Thi Viet Nguyen (Hanoi University of Industry, Vietnam); Cong-Kha Pham (University of Electro-Communications, Japan); Xuan Thanh Pham (Hanoi University of Industry, Vietnam); Kha Manh Hoang (Hanoi University of Industry, Vietnam)	

16:00 - 16:15	Effect of Temperature on the Stability of SnSe Nanoribbons as a Channel Material for Field-Effect Transistors	Nilufer Ertekin (Yalova University, Turkey & The University of Western Australia, Australia); Wen Lei (The University of Western Australia, Australia)	
16:15 - 16:30	A 12-bit 100MS/s SAR ADC with Sub-Radix and Optimize Digital Delay Path	Long Pham Hoang Ho; Lam Thien Van; Cuong Huynh (University of Technology - VNUHCM, Vietnam)	
17:30 - 21:00	**Gala Dinner**		

Day 2: 17 June 2025

Keynote Speech (*Chair: Dr. Duy-Hieu Bui (Information Technoloy Insitute - VNU Hanoi),* Assoc. Prof. Le Duc Hung (The University of Science - VNUHCM))			
08:00 - 08:40	Keynote #3: Photonics Integrated Circuits: Enabling the Next Era of High-Speed, Energy-Efficient Computing	Le Quang Dam (Marvell)	Main hall, I building
08:40 - 09:10	CASS DL Talk: Advanced Circuits and Systems for Navigation-Grade MEMS Accelerometers	Jian Zhao (Shanghai Jiao Tong University, China)	
9:15 - 10:15	**Technical Session: FPGA and Embedded Systems (Chair: Assoc. Prof. Truong Quang Vinh - The University of Technology - VNUHCM)**		
9:15 - 9:30	QEA: An Accelerator for Quantum Circuit Simulation with Resources Efficiency and Flexibility	Van Duy Tran; Tuan Hai Vu; Vu Trung Duong Le; Hoai Luan Pham; Yasuhiko Nakashima (Nara Institute of Science and Technology, Japan)	Main hall, I building
9:30 - 9:45	HW/SW Co-Design for a Variational AutoEncoder targeting Anomaly Detection on FPGA	Tung-Bach Nguyen (University of Engineering and Technology, VNU Hanoi, Vietnam); Tuan-Phong Tran (Phenika University, Vietnam); Thien-Duy Ho (University of Engineering and Technology, VNU Hanoi, Vietnam); Duy-Hieu Bui (Information Technology Institute - VNU Ha noi, Vietnam); Xuan-Tu Tran (Information Technology Institute - VNU Ha noi, Vietnam)	
9:45 - 10:00	Efficient ECG Beat Classification Using Inception Network on Software and FPGA Platforms	Diem Thi Tran; Le Nguyen Nhat Nam (University of Information Technology, VNU-HCM, Vietnam)	
10:00 - 10:15	Analysis of Plant Electrical Signals on an IoT Platform	Xuan Bach Duy Nguyen (University of Information Technology - VNUHCM); Bao Chau Pham Ngoc (University of Information Technology - VNUHCM); Anh-Vu Dinh-Duc (International University - VNUHCM)	
9:15 - 10:30	**Technical Session: Communication, RF and Microwave Circuits (Chair: Dr. Huynh Phu Minh Cuong - The University of Technology - VNUHCM)**		
9:15 - 9:30	A Transformer Feedback Oscillator	Weiwen Lin; Zhiqun Li; Zhennan Li; Yan Yao; Bofan Chen; Muhammad Hashim; Yassin Abdullah (Southeast University, China)	Room I23
9:30 - 9:45	Synthesis of cosecant squared pattern antenna arrays using the methods of stacked beams	Nhu Thai Le; Thanh Cong Vu; Tuan Anh La; Hoai Son Nguyen; Hang Le Thi (Vietel, Vietnam)	
9:45-10:00	Nonlinear Capacitance Compensation Low Noise Amplifier and Mixer with UWB Anchor Antenna	Wen Cheng Lai (National Taiwan University of Science and Technology, Taiwan)	
10:00 - 10:15	Dynamic Queue Management and Packet Loss Mitigation in P4-Enabled Data Planes	Bui Ngoc Thanh Binh; Tran Nguyen Tuan Kiet; Nguyen Viet Ha (University of Science, VNU-HCM, Vietnam)	
10:15 - 10:30	A Data Labeling Method in Deep Learning Model for User Clustering in the NOMA Systems	Ngo Minh Nghia; Nguyen Thi Xuan Uyen; Nguyen Dung; Kha Duy Thai Ngoc; Dang Le Khoa (University of Science, VNU-HCM, Vietnam)	

10:15 - 10:45	**Coffee break**		
10:45 - 11:45	**Technical Session: Digital Circuits and Systems (Chair: Dr. Tran Thi Diem - The University of Information Technology - VNUHCM)**		
10:45 - 11:00	RTL Design of Convolution for CNN Using Baugh Wooley and Wallace Tree Multipliers	Vinh Truong Quang; Quan Doan Duy; Khang Nguyen Minh (University of Technology, VNUHCM - Vietnam)	Main hall, I building
11:00 - 11:15	High-Efficiency 4:2 Compressor Designs: A Comparative Study on Hardware Cost and Error Trade-Offs	Vishnu Padmakumar; Adhiraj Nandy; Sourav Nath; Koushik Guha; Krishna Baishnab; Saroj Biswas (National Institute of Technology Silchar, India)	
11:15 - 11:30	SDR Implemented Algorithm for Real Time Intra-pulse Modulated Radar Signal Analysis	Duong Van Minh (Le Quy Don Technical University, Vietnam & University of Defence, Czech Republic); Duy-Cong Nguyen; Phuong Nguyen; Hoa Quang Nguyen; Giang Phan; Tan Phat Huynh; Manh Long Nguyen (Le Quy Don Technical University, Vietnam	
10:45 - 11:45	**Technical Session: Hardware Security and Cryptography (Chair: Prof. Pham Cong Kha - The University of Electro-Communications, Japan)**		
10:45 - 11:00	DDoS Attack Detection for Software-Defined Network Architecture Based on Artificial Intelligence	Thai-Bao Pham; My Nguyen-Le-Ha; Luan Van-Thien; Thuat Nguyen-Khanh; Quan Le-Trung (University of Information Technology, VNU-HCM, Vietnam)	Room I23
11:00 - 11:15	Solution for Built-in On-chip Hardware Design Integrity Control Adopting resource-optimized RO-PUF	Quang-Kien Trinh (Le Quy Don Technical University, Vietnam); Hoang-Long Nguyen Viettel High Tech, Vietnam; Hoa Quang Nguyen (Le Quy Don Technical University, Vietnam); Tri-Hieu Le (Le Quy Don Technical University, Vietnam); Van-Toan Tran (Le Quy Don Technical University, Vietnam); Duy-Cong Nguyen (Le Quy Don Technical University, Vietnam)	
11:15 - 11:30	Correlation Power Analysis of Pipelined and Multi-Threaded Coarse-Grained Reconfigurable Cryptographic Accelerator	Van-Tuan Luu (Le Quy Don Technical University, Vietnam); Hoai Luan Pham (Nara Institute of Science and Technology, Japan); Van Tinh Nguyen (Le Quy Don Technical University, Vietnam); Van-Phuc Hoang (Le Quy Don Technical University, Vietnam); Nguyen Van Trung (Le Quy Don Technical University, Vietnam); Vu Trung Duong Le (Nara Institute of Science and Technology, Japan); Yasuhiko Nakashima (Nara Institute of Science and Technology, Japan)	
11:30 - 11:45	Data communication security for FANETs using Ascon lightweight cryptography	Huyen-Trang Pham-Thi; Duy-Hieu Bui; Xuan-Tu Tran (Information Technology Institute - VNU Ha noi, Vietnam)	
12:00 - 13:30	Lunch		
13:30 - 15g45	**Special Session on new trends on IC Design and Semiconductor (Chair: Assoc. Prof. Le Duc Hung - The University of Science - VNUHCM)**		
13:30 - 14:15	Advance the development of System-on-Chip and Software-Defined Vehicles architectures for Automotive Electronics Design	Tran Dac Khoa (Renesas)	Main hall, I building
14:15 - 14:45	Spiking Neural Network - A new approach to hardware-based AI designs	Le Trung Khanh (The University of Science - VNUHCM)	
14:45 - 15:15	**Coffee break**		
15:15 - 15:45	UCIe Design and Challenges	Tran The Minh (Synopsys)	
	Closing session	**Dr. Duy-Hieu Bui (VNU Information Technology Institute)**	