Program Guide

The 2026 IEEE 11th International Conference on Integrated Circuits, Design and Verification (ICDV 2026)

October 08 - 10, 2026

Le Quy Don Technical University, Hanoi, Vietnam

Contents

Executive Committee

Steering Co-Chairs
Xuan-Nam Tran, LQDTU, Vietnam
Makoto Ikeda, Uni. of Tokyo, Japan

General Co-Chairs
Xuan-Tu Tran, CASS, Vietnam
Cong-Kha Pham, UEC, Japan
Van-Phuc Hoang, LQDTU, Vietnam

Technical Program Co-Chairs
Koichiro Ishibashi, UTM, Malaysia
Quang-Kien Trinh, LQDTU, Vietnam
Mai-Khanh Nguyen Ngoc, SJSU, United States
Duc-Hung Le, HCMUS, Vietnam

Publication Co-Chairs
Duy-Hieu Bui, VNU-ITI, Vietnam
Huu Hung Nguyen, LQDTU, Vietnam
Dinh Tuan Nguyen, LQDTU, Vietnam
Xuan Thanh Pham, HaUI, Vietnam

Local Arrangement Co-Chairs
Quoc Dinh Nguyen, LQDTU, Vietnam
Quy Thang Bui, LQDTU, Vietnam
Dinh Ha Dao, LQDTU, Vietnam

Special Session Co-Chairs
Anh-Tuan Do, A*STAR, Singapore
Trong-Thuc Hoang, UEC, JP
Thanh Loan Pham Nguyen, HUST

Publicity Co-Chairs
Massimo Alioto, NUS, Singapore
Khanh N. Dang, UoA, Japan
Thanh-Toan Dao, UTC, Vietnam
Hoang Vu Nguyen, LQDTU, Vietnam
Manh Thang Ha, LQDTU, Vietnam

Secretary
Van-Trung Nguyen, LQDTU, Vietnam

Local Information

Hanoi is the antique and dynamic capital of Vietnam. It is the second largest city and also the national hub of commerce, technology science research and culture in Vietnam.

Hanoi is famous for numerous rivers, lakes, and mountains alongside and in the surroundings. It is also well known for typical tropical seasoned place of South East Asia with four seasons: fresh, green and cool in Spring, a bit hot in Summer, fine in Autumn, and cold in Winter.

Hanoi is a harmonious combination of historical, beautiful, and modern landscapes, and friendly residents. In Hanoi, visitors can discover many famous historical sites, e.g., The Literature Temple (a.k.a Van Mieu - Quoc Tu Giam), One-Pillar Pagoda (a.k.a Chua Mot Cot), Lake of Returned Sword (a.k.a Ho Hoan Kiem), Ba Dinh Square, President Ho Chi Minh Mausoleum, etc.

Some typical wonderful places and tours around Hanoi are as follows:

- Halong Bay-on-land and the Citadel (1 day)
- Legendary Hanoi City Tour (1 day)
- Hanoi Art and Craft experience (1 day)
- Fantastic 2 days 1 night Lan Ha Bay Cruise (2 days 1 night)

Temple of Literature

One-Pillar Pagoda

Hoan Kiem Lake (Lake of Returned Sword)

Halong Bay

Ba Dinh Square

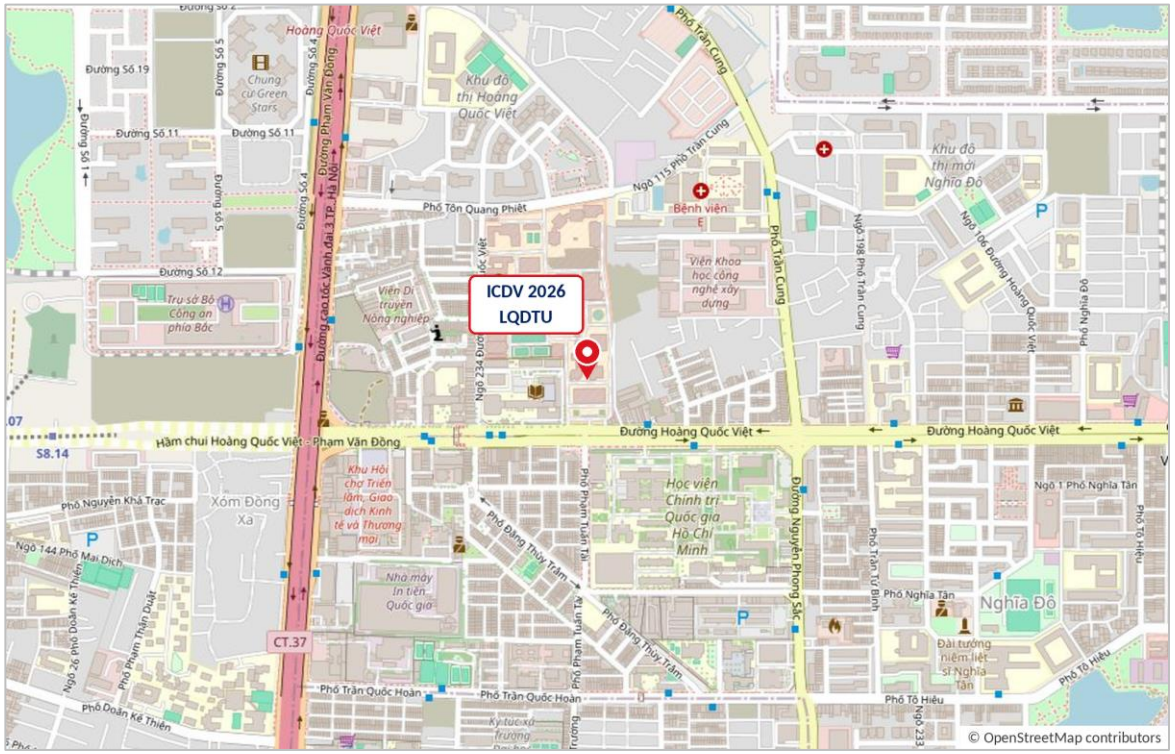
Imperial Citadel of Thang Long

Conference Venue: Le Quy Don Technical University

LE QUY DON TECHNICAL UNIVERSITY

About LQDTU

Le Quy Don Technical University (LQDTU) is one of Vietnam's leading science and technology universities, offering multidisciplinary undergraduate and postgraduate training in engineering and management. LQDTU provides a wide range of highly qualified Bachelor, Master, and Doctoral programs. All academic affairs are led by the Science and Academic Council. Building on our traditions and values over half a century of development, and supported by our highly motivated, intelligent, and enthusiastic academic staff, we ensure LQDTU is a leading center of knowledge in science and technology, delivering excellence in teaching, learning, and research.



Venue

- **Rooms:** Hoan Kiem and Ba Dinh, 5F, S1 building
- **Address:** 236 Hoang Quoc Viet Street, Nghia Do Ward, Hanoi, Vietnam
- **GPS:** 21.0472° N, 105.7864° E

Getting there from Noi Bai International Airport (HAN)

- About 25–30 km north of central Hanoi; 35–60 minutes depending on traffic
- Terminal 2 (T2): international flights; Terminal 1 (T1): domestic flights
- Taxi, Grab, airport shuttle/bus, or hotel-arranged transfer

Scan to open in Google Maps

https://maps.app.goo.gl/rzbDn3CdcBrXDMUw6

Conference website: https://icdv-conf.org

Message from the IEEE ICDV 2026 Chairs

Warmly welcome to the 11th International Conference on Integrated Circuits, Design, and Verification (IEEE ICDV 2026) at Le Quy Don Technical University, Vietnam.

The conference aims to provide a premier forum for exchanging ideas, discussing research results, and presenting chips, circuit designs, and applications in the fields of solid-state and semiconductor technologies. This year, we received 108 submissions from 13 countries. After carefully examining all the received review reports, the conference TPC finally selected only 57 high quality papers for presentation at the conference and publication in the IEEE ICDV 2026 proceedings.

The conference will feature 5 keynotes from renowned world-class leaders in the area including Prof. Bah-Hwee Gwee, Nanyang Technological University, Singapore (will give talk on Next-Generation IC Security); Dr. Sylvain Guilley, Cadence Design Systems and Telecom Paris, France (will give talk on Enforcing Security in the Supply Chain of Chiplets through Transparency); Prof. Kosin Chamnongthai, King Mongkut's University of Technology Thonburi, Thailand (will give talk on Practical Non-Destructive Detection); Prof. Koichiro Ishibashi, Universiti Teknologi Malaysia Kuala Lumpur (UTMKL), Malaysia (will give talk on I Compute-in-Memory at EUV/FINFET Era); and Prof. Makoto IKEDA, Systems Design Lab (D.lab), Engineering School, The University of Tokyo, Japan (will give talk on Hardware Accelerator Design and Optimization for Functional Encryption). This year, the technical sessions feature 3 invited talks and a comprehensive technical programme that spans most state-of-the-art research in all fields of Integrated Circuits, Design, and Verification.

A conference of this size cannot be organized without the hard work and dedication of many people. We would like to thank all authors who submitted their We would like to express our sincere thanks to all sponsors, authors, keynote/invited speakers, session chairs, committee members, and participants to build this memorable and informative conference.

We hope you all enjoy Hanoi and the IEEE ICDV 2026 technical program and find this conference a productive opportunity to explore, exchange ideas, make new friends, and would come back next year to contribute future IEEE ICDV conferences.

Steering Chairs: Xuan-Nam Tran, LQDU, Vietnam; Makoto Ikeda, Uni. of Tokyo, Japan

General Chairs: Xuan-Tu Tran, CASS, Vietnam; Cong-Kha Pham, UEC, Japan; Van-Phuc Hoang, LQDTU, Vietnam.

Technical Program Chairs: Koichiro Ishibashi, UTM, Malaysia; Quang-Kien Trinh, LQDTU, Vietnam; Mai-Khanh Nguyen Ngoc, SJSU, United States; Duc-Hung Le, HCMUS, Vietnam.

Message from LQDTU

Dear scientists, researchers and colleagues!

First of all, on behalf of Le Quy Don Technical University, I would like to welcome all of you to our university to participate in the 11th International Conference on Integrated Circuits, Design, and Verification (IEEE ICDV 2026). I am pleased to know that this event is organized in order not only to serve as a research forum for professors and scientists to introduce new technologies and research achievements but also to boost the collaboration between universities and companies in the field of Integrated Circuits, Design, and Verification. I am very happy to hear that among 108 submitted manuscripts, there are 57 high quality papers selected for presentation at the conference and publication in the conference proceedings. The conference will also feature 5 keynotes and 3 invited talks from renowned world-class leaders in the area. As you may have known, Le Quy Don Technical University is among the national-key universities in Viet Nam and one of the national top universities of science and technology. The university offers multidisciplinary undergraduate and postgraduate education in engineering and management for both civilian students and army officers. Building on our 60 years of experience in engineering education and research, we are committed to contributing to the national semiconductor strategy through high-quality education, advanced scientific research, technological innovation, and international cooperation.

Ladies and gentlemen,

Today, semiconductors are at the heart of artificial intelligence, high-performance computing, autonomous systems, advanced communications, cybersecurity, and virtually every aspect of the digital economy. Vietnam has identified the semiconductor industry as a strategic and foundational technology sector for the country's future development. Le Quy Don Technical University has been selected as one of the 19 higher education institutions prioritized for the development of semiconductor human resources in Vietnam.
Towards a research university, we are conducting various joint research projects with industrial partners as well as research institutions. We have established international collaborations with many foreign partners. Therefore, I do hope that you will enjoy the technical program and find this conference a productive opportunity to explore, exchange ideas, make new friends, and, most importantly, get motivated to return and contribute to future IEEE ICDV conferences.

I would like to express my special thanks to all sponsors, speakers, and elite delegates for your valuable contribution and participation. Finally, I wish you and your families health, happiness, and success!

Sincerely!
Prof. Xuan-Nam Tran
Vice President, LQDTU

Coffee Breaks, Lunch, and Gala Dinner and Presentation Guidelines

- **There will be 4 coffee breaks, 2 lunches, and 1 gala dinner during the two conference days (October 08th and 09th, 2026) as follows:**
  - **Coffee breaks: 10:00 - 10:25 and 14:30 - 14:55 on October 08th; 09:25 - 09:45 and 15:35 - 15:55 on October 09th.**
  - **Lunches: 12:00 - 13:20 on October 08th; 11:50 - 13:10 on October 09th.**
  - **The Gala Dinner will be held from 18:30 to 21:00 on October 08th at Ruby 2 Hall, Trống Đồng Palace, no. 72 Tran Dang Ninh, Nghia Do ward, Hanoi.**
- **Conference venue: 5F, S1 building, Le Quy Don Technical University, 236 Hoang Quoc Viet str., Nghia Do ward, Hanoi, Vietnam.**
- **Time for presentations:**
  - **Keynotes: 30 min for presentation and 5 min for Q&A**
  - **Invited talks: 20 min for presentation and 5 min for Q&A**
  - **Regular papers: 14 min for presentation and 4 min for Q&A**
- **Notes: Please copy your presentation slides to the laptop at the session rooms before your sessions.**

Program at a Glance: Thursday, October 08, 2026

Time (Hanoi)	Room: Hoan Kiem	Room: Ba Dinh
07:30 - 08:30	**Registration**	
08:30 - 08:50	**Opening Session**	
08:50 - 09:25	**Keynote 1: "Next-Generation IC Security: Resilient Hardware Design and AI-Enabled Forensic Verification"** *Prof. Bah-Hwee Gwee, Nanyang Technological University, Singapore*	
09:25 - 10:00	**Keynote 2: "Enforcing Security in the Supply Chain of Chiplets through Transparency"** *Dr. Sylvain Guilley, Cadence Design Systems and Telecom Paris, France*	
10:00 - 10:25	**Coffee break**	
10:25 - 11:55	**R1: Memory, Digital Systems and Testing** (5 papers/90 min)	**R2: AI, IoT & Communications 1** (5 papers/90 min)
12:00 - 13:20	**Lunch**	
13:30 - 14:05	**Keynote 3: "Practical Non-Destructive Detection: Case Study of Durain, Mangosteen, and Granular Ingredients"** *Prof. Kosin Chamnongthai, King Mongkut's University of Technology Thonburi, Thailand*	
14:05 - 14:30	**Invited Talk 1: Bridging the Gap Between Specification and Reality: Cellular Modem Development and Global Field Testing** *Prof. Chaehag Yi, Seoul National University, Korea*	
14:30 - 14:55	**Coffee break**	
14:55 - 16:07	**R3: FPGA and Embedded Systems 1** (4 papers/72 min)	**R4: Analog/Mixed-Signal Circuits 1** (4 papers/72 min)
16:10 - 17:40	**R5: Hardware Security and Cryptography 1** (5 papers/90 min)	**R6: RF, Microwave Circuits and Related Topics** (5 papers/90 min)
18:30 - 21:00	**Gala Dinner**	

Program at a Glance: Friday, October 09, 2026

Time (Hanoi)	Room: Hoan Kiem	Room: Ba Dinh
07:30 - 08:00	**Registration**	
08:00 - 08:25	**Invited Talk 2: "Open-Source EDA and PDKs in VLSI Design: The Era of Agentic AI, Maturing Ecosystems, and Democratized Silicon"** *Prof. Trong-Thuc Hoang, University of Electro-Communications, Japan & Prof. Van-Phuc Hoang, Le Quy Don Technical University, Vietnam*	
08:25 - 08:50	**Invited Talk 3: A Methodology to Derive Security Specifications for Complex Electronic Systems** *Sylvain Guilley (Telecom ParisTech & Secure-IC, France); Ritu-Ranjan Shrivastwa and Ville Yli-Mayry (Secure-IC, France)*	
08:50 - 09:25	**Keynote 4: "From Cloud Datacenters to Secure Edge: Review of Compute-in-Memory at EUV/FINFET Era"** *Prof. Koichiro Ishibashi, Universiti Teknologi Malaysia Kuala Lumpur (UTMKL), Malaysia*	
09:25 - 09:45	**Coffee break**	
09:45 - 11:40	**Invited talk 4: "Phase measuring deflectometry: A full-field and high-accuracy 3D optical metrology technique for advanced packaging process"** (25 min) *Dr. The-Manh Nguyen, Nexensor* **R7: FPGA and Embedded Systems 2** (5 papers/90 min)	**R8: AI, Quantum Tech. & Secure Autonomous UxV Systems** (6 papers/108 min)
11:50 - 13:10	**Lunch**	
13:30 - 14:05	**Keynote 5: "Hardware Accelerator Design and Optimization for Functional Encryption"** *Prof. Makoto IKEDA, Systems Design Lab (D.lab), Engineering School, The University of Tokyo, Japan*	
14:05 - 15:35	**R9: AI, IoT & Communications 2** (5 papers/90 min)	**R10: Analog/Mixed-Signal Circuits 2** (5 papers/90 min)
15:35 - 15:55	**Coffee break**	
15:55 - 17:25	**R11: Semiconductor Technology** (4 papers/72 min)	**R12: Hardware Security and Cryptography 2** (4 papers/72 min)
17:25 - 17:35	**Closing**	

Program at a Glance: Saturday, October 10, 2026

Time (Hanoi)	Room: Hoan Kiem	Room: Ba Dinh
09:30 - 11:00	**Committee Meeting**	

Keynote Speaker #1

Title: Next-Generation IC Security: Resilient Hardware Design and AI-Enabled Forensic Verification

Prof. Bah-Hwee Gwee, Nanyang Technological University, Singapore

Room: Hoan Kiem - Thursday, October 08th, 08:50 - 09:25

Chair: Prof. Xuan Nam Tran, LQDTU

Abstract

Modern integrated circuits face increasingly sophisticated physical and structural attacks across their lifecycle. This keynote presents a closed-loop approach to hardware security that combines proactive, by-design resilience with automated post-silicon forensic verification. The first half of the talk introduces hardware design-for-security techniques that protect against run-time threats. We present an asynchronous AES engine that integrates dual-rail balanced logic for amplitude hiding with stochastic delay lines for time-domain desynchronization, reducing side-channel leakage from transient physical signatures. We also discuss resilient logic locking techniques, including advanced MUX-based approaches such as N-MUX and InvMUX, which mitigate structural leakage exploited by machine learning-driven reverse engineering and IP piracy attacks. The second half focuses on supply-chain trust and post-fabrication verification. We showcase an intelligent forensic pipeline that combines computer vision and generative AI to analyze high-resolution IC microscopy images for circuit-layer segmentation and automated netlist extraction. Hierarchical Graph Neural Networks (GNNs) are then used to identify functional subcircuits without prior layout knowledge, while BERT-style Masked Language Models (MLMs) support firmware provenance analysis and binary code error correction. By integrating hardware-level protection with AI-driven post-silicon verification, this talk highlights a practical pathway toward establishing trustworthy and verifiable next-generation silicon systems.

Biography

Dr. Bah-Hwee Gwee received his B.Eng degree from University of Aberdeen, UK, in 1990. He received his MEng and PhD degrees from Nanyang Technological University in 1992 and 1998 respectively. He been an Associate Professor in NTU since 2005. He is currently the Associate Chair Undergraduate (Students) in School of EEE, NTU and the Director of National Integrated Center for Evaluation, Singapore. He has been the PIs and Co-PIs of a number of research projects including Singapore NRF, DSO, A*STAR, MoE, DSTA, CSA and USA DARPA with research grants amounting to more than US$15m. He has published more than 200 technical papers, 6 granted US patents and 2 Start-up Companies in 2005 and 2020. His areas of research are in hardware assurance, hardware security and post quantum safe cryptography ICs. Dr Gwee was the Chairman of IEEE Circuits and Systems Society (CASS) Singapore Chapter in 2005, 2006, 2013 and 2016. He was the Chairman of IEEE CASS DSP Technical Committee (2019-2020). He was the General Chair of IEEE DSP 2018, IEEE SOCC 2019, IEEE ISICAS 2021 and IEEE ISCAS 2024. He is currently the Chair of the IEEE CAS Society Distinguished Lecturer Program since 2025. He had presented keynotes in IEEE PAINE, IEEE APCCAS, IEEE MCSoC, ICDIS and AIPOSH. He has also served as Associate Editors of several journals, including IEEE CAS Magazine (2021-2022) IEEE T-CAS II (2010-2011, 2018-2019 and 2020-2021) and IEEE T-CAS I (2012-2013). He was an IEEE Distinguished Lecturer in 2009-2010 and in 2017-2018. He was awarded the Singapore Defence Technology Prize (R&D) in 2016.

Keynote Speaker #2

Title: Enforcing Security in the Supply Chain of Chiplets through Transparency
Dr. Sylvain Guilley, Cadence Design Systems and Telecom Paris, France
Room: Hoan Kiem - Thursday, October 08th, 09:25 - 10:00
Chair: Prof. Xuan Tu Tran, VNU ITI

Abstract

In an open market, a massive amount of chiplets will arise from various provenances. How to ascertain that they are genuine? How to ensure that they won't be counterfeited? In this presentation, I will advocate that ecosystem coordination is required. Trust in the chiplets model requires that IP can be traced. Hence, the need for an industry-level transparency in the sourcing. For such a vision to become concrete, chiplets shall be considered as roots of trust. Concrete solutions will be put forward, building on open standards.

Biography

Sylvain Guilley is a fellow at Cadence, within the Silicon Solution Group. Before this position, he was co-founder & CTO at Secure-IC, a company acquired by Cadence Design Systems in 2025. Sylvain is also an adjunct professor at Telecom Paris, and research associate at Ecole Normale Superieure (ENS). He is lead editor of international standards, such as ISO/IEC 20897 (Physically Unclonable Functions), ISO/IEC 20085 (Calibration of non-invasive testing tools), and ISO/IEC TR 24485 (White Box Cryptography). As administrator of Embedded France professional association, he leads the cybersecurity working group. Sylvain has co-authored 350+ research papers and filed 40+ invention patents.

Keynote Speaker #3

Title: Practical Non-Destructive Detection: Case Study of Durain, Mangosteen, and Granular Ingredients

Prof. Kosin Chamnongthai, King Mongkut's University of Technology Thonburi, Thailand

Room: Hoan Kiem - Thursday, October 08th, 13:30 - 14:05

Chair: Prof. Duc Hung Le, HCMUS

Abstract

Many agricultural products such as granular ingredients, durian, mangosteen, and so on need moisture measurement to determine quality. Originally, the moisture inside fruits and granular ingredients are manually measured by percent dry weight which is precise destructive way and takes as long as 24-hour time. Consumers normally prefer non-destructive way which is believed not to destroy agricultural product quality. Technically microwave is sensitive with moisture and selected in this research project to sense moisture for the product quality guarantee. The talk may discuss how to design container and system for granular ingredient, mangosteen, and durian inspection as practical case study.

Biography

Kosin Chamnongthai currently works as a professor at the Electronic and Telecommunication Engineering Department, Faculty of Engineering, King Mongkut's University of Technology Thonburi (KMUTT). He now serves as president-elect of APSIPA Association (2025-2026), and have served as vice president (conference) of APSIPA Association (2020-2023), president of ECTI Association (2018-2019), editor of ECTI e-magazine (2011-2015), associate editor of ECTI-CIT Trans (2011-2016), associate editor of ECTI-EEC Trans (2003-2010), associate editor of ELEX (IEICE Trans) during 2008-2010, and chairman of IEEE COMSOC Thailand (2004-2007). He received a B.Eng. in Applied Electronics from the University of Electro-communications, Tokyo, Japan in 1985, an M.Eng. in Electrical Engineering from Nippon Institute of Technology, Saitama, Japan in 1987, and a Ph.D. in Electrical Engineering from Keio University, Tokyo, Japan in 1991. His research interests include computer vision, image processing, robot vision, signal processing, and pattern recognition. He is a senior member of IEEE, and a member of IEICE, TESA, ECTI, AIAT, APSIPA, TRS, and EEAAT.

Keynote Speaker #4

Title: From Cloud Datacenters to Secure Edge: Review of Compute-in-Memory at EUV/FINFET Era

Prof. Koichiro Ishibashi, Universiti Teknologi Malaysia Kuala Lumpur (UTMKL), Malaysia

Room: Hoan Kiem - Friday, October 09th, 08:50 - 09:25

Chair: Dr. Duy-Hieu Bui, VNU ITI

Abstract

Driven by the massively parallel processing of MAC units in GPUs and the high-bandwidth scaling of memory systems such as HBM, AI training performance has expanded significantly, leading to larger model scales with massive parameter counts. Concurrently, edge devices demand a reduction in circuit area for inference, lower power consumption, and low-bit quantization of integer (INT) and floating-point (FP) data formats to meet form-factor constraints. To achieve the next breakthrough in AI performance against these technological trends, Compute-in-Memory (CIM) and Processor-in-Memory (PIM) technologies have been actively discussed. In FinFET technologies from the 16nm down to the 3nm node fabricated via EUV lithography, matching the gate pitch between 6T SRAM memory arrays and peripheral logic circuits prevents transistor characteristic degradation even when they are placed in close proximity. This enables compact layout areas for CIM/PIM implementations. Furthermore, FinFETs offer excellent saturation characteristics (low drain conductance Gd), a subthreshold slope close to the theoretical limit, and minimal device variation. Leveraging these features alongside dynamic assist circuits, numerous techniques have been proposed to operate both logic and SRAM at the same scaled low voltage. This invited talk provides an overview of recent PIM/CIM technologies, focusing primarily on the cutting-edge innovations discussed in the 16nm to 3nm generations.

Biography

Prof. Koichiro Ishibashi is currently a Professor of Malaysia - Japan International Institute of Technology (MJIIT), Universiti Teknologi Malaysia Kuala Lumpur (UTMKL), Malaysia. He was a full professor of UEC from 2011 to 2023, where he had investigated on low power IoT systems and Energy harvesting technologies for IoT as well as low power LSI design technologies. He has been serving a visiting professor at Ho Chi Minh City University of Technology and Ho Chi Minh City University of Science since 2012. He also serves a visiting professor at Vietnam National University, Information Technology Institute since 2023. After receiving doctor degree from Tokyo Institute of Technology in 1985, he worked at Central Research Laboratory, Hitachi Ltd. and at Renesas Electronics, where he had investigated low power LSI technologies for high density SRAMs and MCUs. He was awarded R&D 100 for the development of SH4 Series Microprocessor in 1999. He has been a Fellow of IEEE from 2005 for the technical contributions to developments of low-power SRAMs and MCUs, and has been a Life Fellow of IEEE since 2024. Throughout his carrier of R&D and education on semiconductor devices and IC designs for 43 Years, he has presented more than 250 academic papers at international conferences and journals including 30 key note or invited presentations. His current interest is educational activities and training on updated semiconductor technologies and IC design techniques, and IoT technologies.

Keynote Speaker #5

Title: Hardware Accelerator Design and Optimization for Functional Encryption

Prof. Makoto IKEDA, Systems Design Lab (D.lab), Engineering School, The University of Tokyo, Japan

Room: Hoan Kiem - Friday, October 09th, 13:30 - 14:05

Chair: Dr. Sylvain Guilley, Cadence Design Systems and Telecom Paris, France

Abstract

This talk covers, hardware accelerator design and optimization of various crypto-algorithms, especially, functional encryption algorithms, including Attribute-based Encryption (ABE). Starting with elliptic-curve and pairing as basis of crypto-algorithms, this talk covers, how to optimize entire functional algorithm implementation in ASIC. This talk also covers, our recent research activities on Agile-X project, which to realize rapid chip design and fabrication.

Biography

Makoto Ikeda received B.E, M.E, and Ph.D. degrees all from Electronic Engineering, the University of Tokyo, in 1991, 1993, and 1996, respectively. He joined the University of Tokyo as a Research Associate in 1996, and is now a Full Professor, in Systems Design Lab.(d.lab), Engineering School, the University of Tokyo. He has been deeply engaged in the VLSI Design and Education Center (VDEC) activities, which is chip design platform for entire Japanese academia, from its foundation of 1996, and is now a director of d.lab, as well as a director of TSMC-Utokyo Lab, and a special advisor to the President of the University of Tokyo. He served a Science Advisor to the Ministry of Education in 2024 and 2025. He served numerous positions in numerous conferences, including ISSCC 2021 ITPC Chair, VLSI Circuits Symposium 2019/17 Symp. and TPC Chairs, A-SSCC 2015 TPC Chair, and ASP-DAC 2027 General Chair. He is now a Vice-President of IEEE Solid-State Circuits Society, and President-Elect of IEICE, Engineering Sciences Society. He is a Senior member of IEEE and Fellow of IEICE.

Invited Talk #1

Title: Bridging the Gap Between Specification and Reality: Cellular Modem Development and Global Field Testing

Prof. Chaehag Yi, Seoul National University, Korea

Room: Hoan Kiem - Thursday, October 08th, 14:05 - 14:30

Chair: Dr. Le Tien Hung, LQDTU

Abstract

As wireless communications evolve from 5G-Advanced toward 6G, the cellular modem remains one of the most sophisticated components in modern communication systems. Its primary challenge is to bridge the gap between 3GPP specifications and the unpredictable behavior of real-world wireless environments. This invited talk provides a comprehensive overview of the modem development lifecycle, from algorithm design and silicon implementation to global field testing and future 6G architectures. The presentation examines the pre-silicon and post-silicon development processes. It introduces the hardware/software co-design of baseband SoCs, together with real-time processor clusters that execute L2/L3 protocol stacks. It also discusses the use of link-level simulators and FPGA-based emulation platforms. The post-silicon phase focuses on silicon bring-up, functional verification, and the transition from laboratory debugging to initial over-the-air calibration. Although conformance testing and channel emulation using commercial test systems are essential for validating compliance with 3GPP standards, they cannot fully reproduce the stochastic behavior of operational mobile networks. Modern field testing which includes drive testing, walk testing, and carrier acceptance testing remains indispensable for commercial deployment. Representative field challenges are also introduced to illustrate why real-world validation remains irreplaceable. We discuss the future evolution of modem engineering for the 6G era. Emerging technologies such as AI-native air interfaces, sub-THz communications, and Non-Terrestrial Networks (NTN) will require a fundamental shift from conventional modem architectures toward AI-assisted adaptive systems. By contrasting deterministic laboratory validation with the complexities of real-world deployment, this presentation provides practical insights into the engineering principles required to design, verify, and optimize next-generation cellular modems.

Biography

Chaehag Yi received the B.S., M.S., and Ph.D. degrees in Electronics Engineering from Seoul National University, Korea, in 1989, 1991, and 1996, respectively. He began his career at ETRI, working on CDMA technology, and later co-founded EoNex, where he developed WCDMA and LTE solutions. During his tenure at Samsung Electronics' System LSI Business, he served as a Vice President, leading the development of smartphone modem chipsets across WCDMA, LTE, and 5G technologies. He joined the Ministry of Science and ICT (MSIT), Korea, where he was in charge of national R&D planning and management in future communications and radio technologies. He is currently a Visiting Professor in the Department of Next-generation Semiconductor Convergence at Seoul National University, teaching semiconductor systems and AI hardware design. His research interests include wireless communications, cellular modem architectures, semiconductor systems and AI hardware design.

Invited Talk #2

Title: Open-Source EDA and PDKs in VLSI Design: The Era of Agentic AI, Maturing Ecosystems, and Democratized Silicon

Prof. Trong-Thuc Hoang, University of Electro-Communications, Japan
& Prof. Van-Phuc Hoang, Le Quy Don Technical University, Vietnam

Room: Hoan Kiem - Friday, October 09th, 08:00 - 08:25

Chair: Prof. Quang Kien Trinh, LQDTU

Abstract

The semiconductor industry continues to experience a profound transformation driven by the open-source hardware movement. Over the past year, the landscape of open-source Electronic Design Automation (EDA) and Process Design Kits (PDKs) has matured rapidly, transitioning from experimental toolchains to robust, community-driven ecosystems. In this talk, we will explore the latest advancements in open-source VLSI design, including the evolution of foundational RTL-to-GDSII flows from OpenLane to LibreLane, and the expansion of accessible fabrication through new open PDKs like IHP 130nm BiCMOS. Furthermore, we will highlight the most disruptive shift in recent EDA research: the integration of Large Language Models (LLMs) and Agentic AI. We will discuss how "language-to-circuit" methodologies and autonomous AI agents are being integrated into platforms like OpenROAD to automate design, alongside recent benchmarking efforts that reveal the ongoing challenges AI faces in optimizing end-to-end Power, Performance, and Area (PPA). Finally, we will examine how these open-source platforms and subsidized tapeout programs are successfully democratizing hardware education, lowering the barrier to entry, and training the next generation of semiconductor engineers to overcome the industry's critical talent shortage.

Biography

Trong-Thuc Hoang received a B.Sc. degree and an M.S. degree in Electronic Engineering from the University of Science (HCMUS), Hochiminh city, Vietnam, in 2012 and 2017, respectively. In 2022, he graduated from the University of Electro-Communications (UEC), Tokyo, Japan, with a Ph.D. degree in Engineering. From 2012 to 2017, he was a lecturer assistant at HCMUS. From 2019 to 2020, he was a research assistant at UEC. From 2019 to 2022, he was a research assistant at the Cyber-Physical Security Research Center (CPSEC), National Institute of Advanced Industrial Science and Technology (AIST), Tokyo, Japan. Since April of 2022, he has been an assistant professor at the Department of Computer and Network Engineering, UEC, Tokyo, Japan. His research interest mainly focuses on digital signal processing, computer architecture, cyber-security, ultra-low power circuit, and system-on-chip.

Van-Phuc Hoang received PhD degree in Electronic Engineering from The University of Electro-Communications, Tokyo, Japan in 2012. He has worked as postdoc researcher, visiting scholar at The University of ElectroCommunications, Tokyo, Japan, Telecom Paris, France and University of Strathclyde, Glasgow, UK during the period of 2012-2018. He is working as an Associate Professor, Director with Institute of System Integration, Le Quy Don Technical University, Hanoi, Vietnam. He is also serving as Vice Chair in International Affairs & Conferences, Radio-Electronics Association of Vietnam (REV). His research interests include hardware security, digital circuits and systems, embedded systems for Internet of Things, and VLSI architecture for digital signal processing. He was the PI of 02 NAFOSTED funded projects and one World Bank funded project in hardware security. He was the Technical Program Chair of several IEEE international conferences such as ICDV 2017, MCSoC 2018, SigTelCom 2019, APCCAS 2020, ATC 2020, ICICDT 2022 and ICD 2026. He is a member of IEEE.

Invited Talk #3

Title: A Methodology to Derive Security Specifications for Complex Electronic Systems

Sylvain Guilley (Telecom ParisTech & Secure-IC, France); Ritu-Ranjan Shrivastwa and Ville Yli-Mayry (Secure-IC, France)

Room: Hoan Kiem - Friday, October 09th, 08:25 - 08:50

Chair: Prof. Trong-Thuc Hoang, University of Electro-Communications, Japan

Abstract

Today's electronic systems are becoming increasingly complex; this challenge comes with demanding PPAs. Consider for instance artificial intelligence chips, aiming at datacenters running LLMs or at automotive perception, which manipulate massive data streams. Let aside performance, those systems are also expected to be more and more dependable. Indeed, when electronic systems are based on chiplets, for instance, the supply chain gets longer and therefore brings a larger number of threats. Also, those systems are very versatile, in that they can run varied multi-tenant applications. Therefore, defining what security features are required in this context with numerous stakes is not trivial. Existing scholarly research is very relevant when the security problem is well defined. The resulting scientific papers accordingly dig very deep: this modus operandi has proved productive in exploring new problems, and actually allowed to come up with innovative solutions. For instance, in the field of side-channel attacks, varied mitigations alongside with metrics to evaluate them have been devised. Increasing sophistication resulted from this research, as external considerations have been injected into the problem (typically, aspects such as attack order, impact of combinatorial glitches, etc.). Therefore, we face today the question of selecting the most suitable technology amongst the state of the art proliferation. In addition, in complex systems, we encounter another problem, namely that of defining the security problem(s). A fruitful approach in this respect is a risk based approach. Specifically, the application of a risk-oriented methodology allows to reason on the security rationale. It proceeds as follows. First, the system missions are listed. Then for each of them, the necessary assets are deduced. A threat analysis allows to identify how assets are threatened, and eventually, security requirements can be enunciated. At this stage, the task of matching relevant countermeasures becomes straightforward. In this paper, we give the example of the security specifications for datacenter and automotive chiplets. The considered missions are (secure) provisioning, trimming, debugging, booting, and remote attestation.

Biography

Sylvain Guilley is a fellow at Cadence, within the Silicon Solution Group. Before this position, he was co-founder & CTO at Secure-IC, a company acquired by Cadence Design Systems in 2025. Sylvain is also an adjunct professor at Telecom Paris, and research associate at Ecole Normale Superieure (ENS). He is lead editor of international standards, such as ISO/IEC 20897 (Physically Unclonable Functions), ISO/IEC 20085 (Calibration of non-invasive testing tools), and ISO/IEC TR 24485 (White Box Cryptography). As administrator of Embedded France professional association, he leads the cybersecurity working group. Sylvain has co-authored 350+ research papers and filed 40+ invention patents.

Invited Talk #4

Title: Phase measuring deflectometry: A full-field and high-accuracy 3D optical metrology technique for advanced packaging process

Dr. The-Manh Nguyen (Nexensor)

Room: Hoan Kiem - Friday, October 09th, 09:45 - 10:10

Chair: Prof. Van-Phuc Hoang, LQDTU

Abstract

The rapid evolution of 2.5D/3D heterogeneous integration, High Bandwidth Memory (HBM), and glass substrates demands unprecedented precision in surface topography and warpage metrology. However, conventional optical inspection techniques face fundamental bottlenecks when evaluating highly specular (mirror-like) surfaces—such as polished die, bare silicon wafers, and Redistribution Layers (RDL). Projection Moiré suffers from severe optical glare on reflective surfaces, while White Light Interferometry (WLI) is constrained by a narrow field-of-view (FOV) and time-consuming axial scanning. To overcome these challenges, this presentation presents Phase-Measuring Deflectometry (PMD) as a non-contact, full-field, and high-accuracy optical metrology framework tailored for advanced semiconductor packaging. PMD projects phase-shifted sinusoidal fringe patterns onto the specular surface and analyzes the reflected distorted patterns to measure local surface gradients with microradian angular sensitivity. By exploiting the law of reflection—where surface tilt angles are doubled in the reflected beam—PMD achieves sub-micron topographical resolution across an entire 300mm wafer in a single inspection cycle without mechanical stage scanning.

Biography

The-Manh Nguyen received B.E degree in Electronics and Telecommunication Engineering from Hanoi University of Science and Technology, Ha Noi, Vietnam, in 2013. He also received Ph.D degree in Measurement Science department with the University of Science and Technology, Daejeon, South Korea, in 2022. He is currently working as Postdoc researcher in Length and Dimensional Metrology Group, Korea Research Institute of Standards and Science, Daejeon, South Korea, from 2022.

Conference Schedule Details

Room: Hoan Kiem - R1: Memory, Digital Systems and Testing

Chairs: Dr. Duy-Hieu Bui, VNU ITI & Dr. Nguyen Hieu, PTIT

Thursday, October 08th, 10:25 - 11:55

Time	Title	Authors
10:25	A Method for Automated Test Input Generation on Verilator-Generated RISC-V Processor Models	Hiếu Đức Vũ (Vietnam National University Hanoi, Vietnam); Duc-Anh Nguyen and Pham Ngoc-Hung (VNU University of Engineering and Technology, Vietnam)
10:43	Algorithm-First NPU Extension via Dual-LLM Workflow	Hsin-I Wu (DeepMentor, Taiwan); You-En Wu (National Yang Ming Chiao Tung University, Taiwan); Ruei-En Wu (Taipei Municipal Heping High School, Taiwan)
11:01	PEARL: Credit-Aware Minimal-Adaptive Routing for Mesh NoC	Tien-Hieu Le (Vietnam National University, Hanoi, Vietnam & Microelectronics and Computer Sciences (MCS) Research Center, N.A Viet Nam Ltd, Nghe An, Vietnam); Duy-Hieu Bui (Vietnam National University, Hanoi, Vietnam); Xuan-Tu Tran (VIetnam National University, Hanoi, Vietnam)
11:19	Optimization-Guided Traffic Generation: Discovering AXI4 Bottlenecks in Edge CNN Accelerators	Hieu Nguyen (PTIT University, Vietnam); Thao Viet Vuong (Posts and Telecommunications Institute of Technology, Vietnam & PTIT, Vietnam); Huyen Thanh Dao (Posts and Telecommunications Institute of Technology, Vietnam & Gunma University, Vietnam); Dao Anh Vu and Minh-Tuan Le (Posts and Telecommunications Institute of Technology, Vietnam)
11:37	A Low-Power and Compact Dynamic Matching and Comparator Circuit with Early Termination for Memory-Centric Computing	Linh Le, Dinh Ha Dao, Kien Trinh Quang, Thi-Hong-Tham Tran and Khoa-Sang Nguyen (Le Quy Don Technical University, Vietnam)

Conference Schedule Details

Room: Ba Dinh - R2: AI, IoT & Communications 1

Chairs: Dr. Xuan Truong Nguyen, SNU, Korea & Dr. Dao Thi Nga, LQDTU

Thursday, October 08th, 10:25 - 11:55

Time	Title	Authors
10:25	3D Maneuvering Target Tracking Algorithm Using Unscented Kalman Filter and Particle Filter	Ngo Nhat Anh (Hanoi University of Science and Technology, Vietnam); Hoang Manh Thang (Hanoi University of Science and Technology (HUST), Vietnam)
10:43	A Dual-Stream Multi-Scale Fusion Network with YOLO-Style Design for Infrared and Visible Images	Shang-Yin Yu, Bo-En Wei and Tsung-Han Tsai (National Central University, Taiwan)
11:01	A Fully-Integrated Raman and Autofluorescence Benchtop System with On-Device AI for Sub-Second Skin Cancer Screening	Hoang ChuDuc (The VNU University of Engineering and Technology & National Technology Innovation Fund, Vietnam)
11:19	Action-Responsive Contrastive Network for Efficient Joint-based Hand Gesture Recognition	Duy Tien Le (Vietnam National University, Hanoi, Vietnam); Dinh-Tan Pham (International School, Vietnam National University, Hanoi, Vietnam)
11:37	An Always-On Screening and Event-Triggered CNN-LSTM Architecture for Low-Power Wearable Fall Detection	Anh Vu-Duc and Thanh Ta-Van (Posts and Telecommunications Institute of Technology, Vietnam); Bien Nguyen Quang and Duan Luong-Cong (Posts and Telecommunications Institute of Technology (PTIT), Vietnam)

Conference Schedule Details

Room: Hoan Kiem - R3: FPGA and Embedded Systems 1
Chairs: Dr. Tran Thi Hong Tham & Dr. Vu Hoang Gia, LQDTU
Thursday, October 08th, 14:55 - 16:07

Time	Title	Authors
14:55	Optimizing Quartznet and Conformer Models for Real-Time Vietnamese Speech Recognition on Edge Devices for Autonomous Vehicles	Thanh-AN Luong (Vietnam National University, Hanoi, Vietnam); Huyen-Trang Nguyen-Thi (The University of Da Nang, Vietnam); Duy-Hieu Bui (Vietnam National University, Hanoi, Vietnam); Xuan-Tu Tran (VIetnam National University, Hanoi, Vietnam)
15:13	A Lightweight, High-Throughput True Random Number Generator on FPGA Using an RTL-Optimized Elias Extractor	Hieu Nguyen (PTIT University, Vietnam); Hop Quynh Pham (Posts and Telecommunications Institute of Technology, Vietnam); Huyen Thanh Dao (Posts and Telecommunications Institute of Technology, Vietnam & Gunma University, Vietnam)
15:31	A Portable Field-Inspection Workflow for Color- and Structure-Faithful Enhancement of PCB Photographs on SBC	Le Tien Hung, Nguyen Huu Tho and Nguyen Le Van (Le Quy Don Technical University, Vietnam)
15:49	Dual-Head Incremental Object Detection on Embedded Vision Platforms	Tsung-Han Tsai and Yao-Chieh Tseng (National Central University, Taiwan)

Conference Schedule Details

Room: Ba Dinh - R4: Analog/Mixed-Signal Circuits 1

Chairs: Pham Xuan Thanh, HaIU & Dr. Huu-Tho Nguyen, LQDTU

Thursday, October 08th, 14:55 - 16:07

Time	Title	Authors
14:55	A 16 Gbps High-Speed Receiver with Active-Inductor-Based Continuous-Time Linear Equalizer on 14nm CMOS Process	Lê Nguyễn Lam Trường (The University of Science, Ho Chi Minh City, Vietnam); Trần Đức Hồng Quân (Synopsys Vietnam, Vietnam); Nguyen Vu Nhat Hoang (Synopsys Viet Nam, Vietnam); Hung Le Duc (University of Science, VNU-HCM, Vietnam)
15:13	A Dual-Channel 6-bit 10-GS/s DAC Design for Driving Forward-Biased MZMs in PNN Prototyping Using 7-nm FinFET Technology	Pradyumna Vellanki (National Sun Yat-Sen University, Taiwan); Chen-Wei Yen (National Sun Yat-sen University, Taiwan); L S S Pavan Kumar Chodisetti and Chua-Chin Wang (National Sun Yat-Sen University, Taiwan)
15:31	A Flipped Voltage Follower Based Capacitor-less LDO with gm-Feedforward Compensation and Slew-rate Enhancement	Minh-Tuan Nguyen (VNU University of Engineering and Technology, Vietnam); Duong Huu-Truong and Mai-Huong Nguyen Thi (Vietnam National University Hanoi, Vietnam); Tuan Anh Mai (VNU University of Engineering and Technology, Vietnam); Linh Mai (University of Engineering and Technology, VNU-Hanoi & UET, Vietnam)
15:49	A P-SSHI Interface for Piezoelectric Energy Harvesting with an Output-Power-Evaluation MPPT Achieving 98.8% MPPT Efficiency	Zhongxin Ye, Rui Zhang and Jianping Guo (Sun Yat-sen University, China)

Conference Schedule Details

Room: Hoan Kiem - R5: Hardware Security and Cryptography 1

Chairs: Dr. Dam Duc Thuan & Dr. Thai-Ha Tran, LQDTU

Thursday, October 08th, 16:10 - 17:40

Time	Title	Authors
16:10	A DWT-SVD Color Image Watermarking Scheme with Wavelet-GAN-Based Chrominance Reconstruction for Side-Information Reduction	Phuong Nguyen Thu and Thanh Ta Minh (Le Quy Don Technical University, Vietnam)
16:28	A High-Speed, Constant-Time, and Memory-Efficient TRNG-Based Sampler for Hamming-Quasi Cyclic KEM	Duc-Thuan Dam (The University of Electro-Communications, Japan); Nguyen Huu Tho (Le Quy Don Technical University, Vietnam); Hung Le Duc (University of Science, VNU-HCM, Vietnam); Cong-Kha Pham (University of Electro-Communications (UEC), Japan)
16:46	A Sub-3.82% Native BER Strong PUF Using Power-Gated Diode-Clamped Inverter Chain and Auto-Stabilizing Mechanism in 28nm CMOS	Trung Tien Hoang (Hanoi University of Science and Technology, Vietnam); Dinh Quoc Bao Tran (Chungbuk National University, Korea (South) & ChungBuk National University, Korea (South)); Van Truong Nguyen (Chungbuk National University, Korea (South)); Loan Pham-Nguyen (Hanoi University of Science and Technology & School of Electronics and Telecommunications, Vietnam); Jong-Phil Hong (Chungbuk National University, Korea (South))
17:04	An Area-Efficient Polynomial Arithmetic for HQC	Nguyen Tien Hung, Nguyen Huu Tho, Hai Thanh Mai and Quang Nguyen-The (Le Quy Don Technical University, Vietnam); Duc-Thuan Dam (The University of Electro-Communications, Japan)
17:22	Hardware-Enforced Security Architecture for Multi-Core RISC-V Systems with Network-on-Chip	Tri-Duc Ta (University of Sciences, VNU-HCM, Vietnam); Van-Quang Vu, Trong-Qui Nguyen, Anh-Quan Le and Nhat-Quang Le (The University of Information Technology, Vietnam); Cong-Kha Pham (University of Electro-Communications (UEC), Japan); Hung Le Duc (University of Science, VNU-HCM, Vietnam)

Conference Schedule Details

Room: Ba Dinh - R6: RF, Microwave Circuits and Related Topics

Chairs: Dr. Huu-Tho Nguyen & Dr. Van Trung Nguyen, LQDTU

Thursday, October 08th, 16:10 - 17:40

Time	Title	Authors
16:10	A 20.2-28 GHz Wide-Tuning Low-Power CMOS LC-VCO with Push-Push Frequency Doubler for FMCW Radar Applications	Juan Salvador (San Jose State University, USA); Mai-Khanh Nguyen (University of Nevada, Las Vegas, USA)
16:28	A Wideband Low-Power CMOS Active Mixer with Current-Reused RF Transconductance Enhancement	Khai Van Mai and Tuan Anh Mai (VNU University of Engineering and Technology, Vietnam); Linh Mai (University of Engineering and Technology, VNU-Hanoi & UET, Vietnam)
16:46	Compact Quad-Band BPF Based on Four-Stage Folded Open-Loop SIRs for Sub-6 GHz Applications	Thang Van Nguyen (Vietnam National University Hanoi, Vietnam); Cuong Quoc Vuong (Vietnam National University, Vietnam); Nguyen Khanh Huyen (VNU University of Engineering and Technology, Vietnam); Thien Minh Nguyen and Duong Nguyen (International University, Vietnam); Tuan Anh Mai (VNU University of Engineering and Technology, Vietnam); Linh Mai (University of Engineering and Technology, VNU-Hanoi & UET, Vietnam)
17:04	A 6 Bit 35-38 GHz Passive Vector-Sum Phase Shifter With Sub-1◦ RMS Phase Error	Dinh-Hung Le and Kim Van Phan (Ho Chi Minh City University of Technology, Vietnam); Sanghun Lee (WAVE PIA, Korea (South)); Cuong Huynh (Ho Chi Minh City University of Technology, Vietnam)
17:22	On the Thermal and Voltage Stability of DLS-like Ultra-low-power Ring Oscillators	Dinh Quang Anh (Le Quy Don Technical University, Vietnam); Orazio Aiello (University of Genova, Italy); Van-Phuc Hoang (Le Quy Don Technical University, Vietnam)

Conference Schedule Details

Room: Hoan Kiem – R7: FPGA and Embedded Systems 2

Chairs: Prof. Dang N. Khanh, UoA, Japan & Dr. Hieu Nguyen, PTIT

Friday, October 09th, 10:10 - 11:40

Time	Title	Authors
10:10	FPGA-based CNN Accelerator for Low-Latency Object Detection Using an Enhanced Systolic Array	Luu Nguyen-Van (Hanoi University of Science and Technology, Vietnam); Nguyen D. Minh (HUST, Vietnam); Xuan Truong Nguyen (Seoul National University, Korea (South)); Dung Viet Do and Linh Nguyen-Thi-Thuy (Hanoi University of Science and Technology, Vietnam); Chi Hoang Phuong (HUST, Vietnam)
10:28	MRCA 3.0: Concurrent Post-Quantum and INT8 AI Execution on a Multi-grained Reconfigurable Accelerator	Long Hau Huynh and Tung Lam Truong (Ho Chi Minh City University of Technology and Engineering, Vietnam); Hoai Luan Pham (NARA Institute of Science and Technology, Japan); Huan Minh Vo (Ho Chi Minh University of Technology and Engineering, Vietnam)
10:46	Novel High-Speed Pedestrian Detection Using Motion Detection and Object Tracking to Support High-Resolution Video Stream on FPGA	Tuan-Phong Tran (Phenika University, Vietnam); Nam Van Dinh (Phenikaa University, Vietnam); Linh Ngoc Nguyen (VNU International School, Vietnam); Duy-Hieu Bui (Vietnam National University, Hanoi, Vietnam); Xuan-Tu Tran (VIetnam National University, Hanoi, Vietnam)
11:04	Predicting Feasibility and Runtime of Randomized PCA-SVD on Single-Board Computers	Le Tien Hung, Nguyen Le Van and Nguyen Huu Tho (Le Quy Don Technical University, Vietnam)
11:22	Radar Pulse Descriptor Word Extraction on RFSoC	Hoang-Gia Vu and Viet-Anh Nguyen-Van (Le Quy Don Technical University, Vietnam); Tuan Khang Nguyen (Center 80 of Electrical Engineerings, Vietnam); Nguyen Tuan (Le Quy Don Technical University, Vietnam)

Conference Schedule Details

Room: Ba Dinh – R8: AI, Quantum Tech. & Secure Autonomous UxV Systems

Chairs: Prof. Ta Minh Thanh & Dr. Pham Truong Son, LQDTU

Friday, October 09th, 09:45 - 11:33

Time	Title	Authors
09:45	AI-Enabled Autonomous UxV Navigation via Multi-Sensor Fusion and Risk-Aware Decision Making	Trung Thi Hoa Trang Nguyen and Toan Dao (University of Transport and Communications, Vietnam); Binh Ngo, Thanh (University of Transport and Communications & UTC, Vietnam); Sy Dieu Nguyen (University of Transport and Communications, Vietnam)
10:03	Component-wise AST Similarity Metric for Evaluating Text-to-Spatial SQL Models	Thai Hung Vo (Academy of Military Science and Technology, Vietnam); Thanh Chi Nguyen (Institute of Military Science and Technology, Hanoi, Vietnam); Le Thi Thu Hong (Military Institute of Science and Technology & MIST, Vietnam)
10:21	HART: Hardware-Aligned Robust Training for Resource-Constrained Edge Device	Chao-Wei Chang, Ya-Chi Peng, Yun-Hao Yang, Wan-Jung Chen and An-Yeu Wu (National Taiwan University, Taiwan); Mladen Berekovic (Universität zu Lübeck, Germany); Shih-Hsu Huang (Chung Yuan Christian University, Taiwan)
10:39	RAFT-SF: Risk-Aware Formation Planning with Safety Filtering for UAV Swarms	Duong Van Dan and Thanh Ta Minh (Le Quy Don Technical University, Vietnam)
10:57	APEG-QIM: Blind Quantum Image Watermarking with Block-Size Optimization for Robustness	Tuat Dao Ngoc (Thai Nguyen University of Information and Communication Technology, Vietnam); Thanh Ta Minh (Le Quy Don Technical University, Vietnam); Trung-Nghia Phung (Thai Nguyen University of Information and Communication Technology, Vietnam)
11:15	Low-Cost Real-Time 3D Environment Perception Using Monocular Depth Estimation on Edge NPU	Quoc-Dat Tran, Duy-Hieu Bui and Xuan-Tu Tran (Vietnam National University, Hanoi, Vietnam)

Conference Schedule Details

Room: Hoan Kiem - R9: AI, IoT & Communications 2

Chairs: Dr. Bui Quy Thang, LQDTU & Dr. Xuan Truong Nguyen, SNU, Korea

Friday, October 09th, 14:05 - 15:35

Time	Title	Authors
14:05	An Efficient Edge-Device Implementation of 2D ECG Classification Based on the Stockwell Transform and Lightweight Swin Transformer	Thanh-Bao Ho, Minh-Thien Nguyen and Minh-Quang Nguyen (HCMUS, Vietnam); Huu-Thuan Huynh (Ho Chi Minh City - University of Science, Vietnam)
14:23	Codebook-Based Synaptic Weight Compression for Spiking Neural Networks	Atharv Sharma and Khanh N. Dang (University of Aizu, Japan)
14:41	Improving Hyperdimensional Regression Through Encoder Redesign and Data Augmentation	Sy-Quyen Nguyen (Le Quy Don Technical University, Vietnam); Thi-Nhan Pham (Hanoi University of Science Technology, Vietnam); Quang-Manh Duong, Thi-Nga Dao and Kien Trinh Quang (Le Quy Don Technical University, Vietnam)
14:59	Mamba-MK: An Implementation of Mamba Decoding Using a Cooperative Megakernel on Consumer and Edge GPUs	Trinh Thi My Linh (Hanoi University of Science and Technology, Vietnam); Chi Hoang Phuong (HUST, Vietnam); Xuan Truong Nguyen (Seoul National University, Korea (South)); Nguyen D. Minh (HUST, Vietnam)
15:17	A lightweight multi-channel CNN for low-latency automatic modulation classification with over-the-air SDR validation	Duong Van Minh (Le Quy Don Technical University, Vietnam & University of Defence, Czech Republic); Giang Phan, Phuong Nguyen, Nguyen Van Dat, Nguyen Van Toi and Pham Trong Hung (Le Quy Don Technical University, Vietnam)

Conference Schedule Details

Room: Ba Dinh - R10: Analog/Mixed-Signal Circuits 2

Chair: Dr. Van-Trung Nguyen & Dr. Huu-Tho Nguyen, LQDTU

Friday, October 09th, 14:05 - 15:35

Time	Title	Authors
14:05	Adaptive Coincidence Detection with Ambient Photon Statistics for Noise Filtering of d-SiPM-based d-ToF Sensor	Lei Shao, Derun Li and Jianping Guo (Sun Yat-sen University, China)
14:23	Foreground Digital Calibration Technique for 14-bit ADC Design Used in PNN Prototyping	L S S Pavan Kumar Chodisetti (National Sun Yat-Sen University, Taiwan); Yen-Jung Lin (National Sun Yat-sen University, Taiwan); Pradyumna Vellanki (National Sun Yat-Sen University, Taiwan); U-Fat Chio (Chongqing University of Posts and Telecommunications, China); Friedel Gerfers (Technical University Berlin, Germany); Chua-Chin Wang (National Sun Yat-Sen University, Taiwan)
14:41	Fully Integrated Inductorless Charge Pump for Energy Harvesting Down to 125 mV	Lucas Ott (Technische Universität Dresden, Germany); Jens Wagner (Technische Universität Dresden & Chair for Circuit Design and Network Theory, Germany); Florian Protze and Frank Ellinger (Technische Universität Dresden, Germany)
14:59	Co-optimized biasing and ADC architecture for substrate temperature compensation in uncooled IR ROICs	Duong Huu-Truong (Vietnam National University Hanoi, Vietnam); Minh-Tuan Nguyen (VNU University of Engineering and Technology, Vietnam); Mai-Huong Nguyen Thi (Vietnam National University Hanoi, Vietnam); Linh Mai (University of Engineering and Technology, VNU-Hanoi & UET, Vietnam); Tuan Anh Mai (VNU University of Engineering and Technology, Vietnam)
15:17	Device-Aware Design and Evaluation of an Ancilla-Assisted Photonic CZ Gate Using Real Mach-Zehnder Interferometer Transfer Matrices	Vu Le Ha (Academy of Science and Technology for Military, Vietnam); Hong Thu Thi Luu (Institute of Electronics, Vietnam); Thanh Cong Pham and Thai Nguyen (AMST, Vietnam)

Conference Schedule Details

Room: Hoan Kiem - R11: Semiconductor Technology

Chairs: Dr. Nguyen Tien Anh & Prof. Van-Phuc Hoang, LQDTU

Friday, October 09th, 15:55 - 17:25

Time	Title	Authors
15:55	Multi-Cell TCAD Analysis of Parasitic-Bipolar-Effect-Induced Multiple-Cell Upsets in a 12-nm FinFET SRAM	Ryuichi Yasuda (Kyoto University, Japan); Koichi Fukuda and Junichi Hattori (National Institute of Advanced Industrial Science and Technology, Japan); Kozo Takeuchi (Japan Aerospace Exploration Agency, Japan); Yuibi Gomi and Masanori Hashimoto (Kyoto University, Japan)
16:13	Phase-Informed Machine Learning for In-Sn-Cu Low-Temperature Solder Alloys: CALPHAD Augmentation, Gaussian Process Regression With Physics, and SHAP-Derived Design Rules	Anh The Vu (Hanoi University of Science and Technology, Vietnam); Chau Van Tran (Le Quy Don Technical University, Vietnam); Han Le Duy (Hanoi University of Science and Technology, Vietnam)
16:31	A Line-Based Adaptive Body-Bias Framework for Low-Power SRAM in 22FDX Technology	Lingfan Zhang and Bah Hwee Gwee (Nanyang Technological University, Singapore, Singapore)
16:49	Physics-Guided Latent-Space Enhancement for Lift-off-Robust Pulsed Eddy Current Corrosion Imaging	Ngo Tung Duong, Ba Long Nguyen, Thang Nguyen Trong and Pham Phuong Huy (Phenikaa University, Vietnam)

Conference Schedule Details

Room: Ba Dinh - R12: Hardware Security and Cryptography 2

Chairs: Dr. Thai-Ha Tran, LQDTU & Dr. Dam Duc Thuan, LQDTU

Friday, October 09th, 15:55 - 17:25

Time	Title	Authors
15:55	An Efficient SoC-FPGA Based Architecture for the Latest ASCON Lightweight Cryptography with Hardware-Software Co-Design	Minh-Thien Nguyen (HCMUS, Vietnam); Bao Thuong T Cao (University of Science, VNU-HCM, Vietnam); Thanh-Bao Ho and Minh-Quang Nguyen (HCMUS, Vietnam); Cong-Kha Pham (University of Electro-Communications (UEC), Japan); Huu-Thuan Huynh (Ho Chi Minh City - University of Science, Vietnam)
16:13	An FPGA-Based ECDSA P-256 Key Generation Accelerator with Integrated TRNG	Phuc-Phan Duong (The University of Electro-Communications, Japan); Thanh Ngoc and Hieu Minh Nguyen (Academy of Cryptography Techniques, Vietnam); Trong-Thuc Hoang (The University of Electro-Communications, Japan); Ngoc-Quynh Chu-Thi (Academy of Cryptography Techniques, Vietnam)
16:31	Application - Specific Integrated Circuit (ASIC) Implementation of Blowfish Algorithm with Optimized Round and S - Box for Enhanced Performance Using Skywater 130 nm CMOS Process	Agustin G. Carillo, Rommel J. Gumata and Re-Ann Cristine O. Calimpusan (Caraga State University, Philippines); Anastacia B Alvarez (University of the Philippines Diliman, Philippines); Angelo T. Batausa (Caraga State University, Philippines)
16:49	FPGA-Based Hardware/Software Co-Design for Modular Reduction and Polynomial Vector Arithmetic in Dilithium scheme	Nhu-Quynh Luc, Phan Cong-Tien-Doan, Nguyen Hai-Long and Nguyen Gia-Bao (Academy of Cryptography Techniques, Vietnam); Thang Nguyen and Toan Dao (University of Transport and Communications, Vietnam)

Notes

Notes


1966
2026
LE QUY DON TECHNICAL UNIVERSITY
60TH ANNIVERSARY
1966 - 2026